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STUDY OF ELECTRONIC TRANSPORT AND BREAKDOWN IN THIN INSULATING FILMS

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Recent progress is reported in an ongoing program of studies of high-field effects in thin insulating films on semiconducting substrates. The investigations reported here include the high-field generation of electron traps in SiO_2, the high field generation of interface states in the $Si-SiO_2$ system, the influence of holes at the interface and the effects of temperature on interface-state generation in the $Si-SiO_2$ system, and studies of high-field effects in the $Si-Al_2O_3$ system.

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1. INTRODUCTION

We report here on recent progress in an ongoing program of research directed toward a basic understanding of the electronic properties of thin insulating films and of the interfaces of such films with semiconductors and metals. Of particular interest are the high-field properties, including charge-carrier injection through the interfaces, electronic transport through the insulator, charge-carrier trapping and recombination at the interfaces and in the insulator, the high-field generation of interface states and trapping centers, and the mechanisms leading to dielectric breakdown. The objective of the program is to provide a rational basis for the choice of materials, processing methods and treatment of the insulating films in order to obtain the desired performance and reliability. The insulating films under study at the present time are silicon dioxide, aluminum oxide, and silicon nitride on silicon substrates. The techniques and apparatus that we have developed under this program are, moreover, immediately applicable to the study of other types of insulating films and substrates.

We have previously reported on our discovery that deep electron traps are generated in thermally grown silicon dioxide under high field conditions[2] and on our studies of the properties of the generated traps.[1,2] The high-field generation of electron traps in SiO_2 may have important consequences in the short-channel MOS transistors now under development by industry and in the operation of dual-dielectric nonvolatile memories utilizing thin films of SiO_2 adjacent to the silicon substrates. In Ch. 2 of this report, C. S. Jenq describes the results of a further investigation of this phenomenon, and shows evidence that the trap generation is a bulk, rather than an interface, phenomenon. The high-field generation of interface states in the MOS system is of concern also, and in Ch. 2 Mr. Jenq gives his recent results on this subject. Mr. Jenq's work has required many of his measurements to be made at liquid nitrogen temperature, both to avoid ionic motion and to inhibit the immediate generation of interface states under high-field conditions,[1] and this has required the development of a method for measuring interface-state densities at these lowered temperatures. His basic method was described in a previous report,[1] and in the present report he shows an extension of his technique to a determination of the energy distribution of the states.

In a previous report,[1] J. J. Clement described his investigation of interface-state generation in MOS structures; in particular the influence of holes at the interface and the effects of temperature on the generation rate. He uses soft X-rays to produce hole-electron pairs in the oxide at liquid nitrogen temperature. The electrons, which have good mobility, are swept out quickly by a moderate electric field, leaving the holes behind. The holes can then be transported to either interface by application of a larger electric field together with excitation by visible light. He finds that although the presence of holes is necessary to start the interface-state generation process, the states do not appear until the sample is warmed. Furthermore, and more surprisingly, if the holes at the interface are recombined with electrons before the sample is warmed, the interface states nevertheless appear as the temperature of the sample is increased. Only the temporary presence of holes is apparently necessary to germinate the interface-state generation process. The results reported previously were all obtained on steam-grown oxides, and it was important to determine whether dry-grown oxides would exhibit a similar phenomenon. In the present report, Mr. Clement describes the results of his study of dry-grown oxides and shows that similar effects do, indeed, take place in these. He gives new results on the temperature dependence of the interface-state generation and he shows the results of measurements of the energy distribution of the states.

S. S. Li is studying high field effects in chemically vapor deposited (CVD) aluminum oxide films on silicon substrates, and he describes his recent results in Ch. 4. Trap-assisted tunneling appears to be the dominant mechanism of charge-carrier injection from the electrodes. Electron trapping occurs through the bulk of the oxide. Positive charging also occurs, and appears to be concentrated near the positive electrode. Mr. Li finds evidence for thermally activated hopping as a mechanism of transport of electrons through the bulk of the oxide. Impact ionization seems not to be an important factor in the dielectric breakdown of CVD Al_2O_3. The instability that precedes breaking appears instead to be determined by charge trapping, possibly together with field-assisted detrapping.

In a companion study to Mr. Li's, O. Bar-Gadda is applying additional techniques to the study of high-field effects in CVD Al_2O_3 on silicon substrates. By use of a bridge circuit which balances out the displacement current in the MOS capacitor he has succeeded in making unusually reliable measurements of the voltage dependence of the current injected into the insulator from the contacts. He has also studied the time evolution of the current over a range of applied voltages. By applying a reasonable first-order model of electron trapping to his experimental results, he finds that trapping occurs through much of the bulk of his oxides. In addition, he presents optical and scanning electron micrographs of breakdown regions.

2. HIGH FIELD EFFECTS IN MOS CAPACITORS
(Ching-Shi Jenq collaborating)

2.1. Introduction

In the preceding Semi-Annual Report[1] we described a new method for measuring interface state densities in MOS capacitors at low temperatures. Originally designated the low-temperature ledge (LTL) method, we now term this the low-temperature C-V displacement (LTD) method, the latter name being considered more descriptive of the technique. As previously described, the LTD method gave the number of interface states in the central region of the substrate bandgap from C-V measurements made at a single low temperature. In Sec. 2.2(A) we describe an extension of the LTD method to the determination of the energy distribution of the interface states in roughly the half of the band gap adjacent to the majority carrier band edge. The latter method requires measurements to be made over a range of (low) temperatures. In Sec. 2.2(B) we discuss difficulties that are sometimes encountered in applying the LTD method.

In Semi-Annual Technical Report No. 2[2] we presented evidence that electron traps are generated in the silicon-dioxide insulators of MOS capacitors when the insulators are stressed with a sufficiently large electric field, and in Report No. 3[1] we discussed some of the properties of these traps. In Sec. 2.3 of the present report we give results indicating that the trap generation is a bulk effect rather than an interface effect, and in Sec. 2.4 we show results on the electric-field dependence of the electron-trap concentration. In Report No. 3[1] we discussed the high-field generation of interface states in the MOS system, and this discussion is continued in Sec. 2.5 of the present report. Results are summarized in Sec. 2.6.

2.2. Further Discussion of the LTD Method of Determining Interface State Densities

2.2(A) Determining Energy Distribution of Interface States

The main advantage of the LTD method[1,3] is that it allows one to measure, at a single low temperature, the total number of interface states over a large portion of the bandgap of Si. Information about the energy distribution of the interface states can not be obtained, however, unless the sample temperature is varied. In the following we present a method

of using the LTD technique to find the energy distribution of interface states in roughly the half band gap adjacent to the majority carrier band. This method might be taken as similar to the Gray-Brown method,[4] but it utilizes different concepts. The difference between the two methods will be mentioned at the end of this section.

We shall write the equations for an n-type substrate. The time constant for emission of electrons from interface states is related to temperature by the following equation:[5]

$$\tau_{en} = \frac{1}{v_{th}\sigma n_i} \exp(E_i - E_s)/kT \qquad (2.1)$$

where v_{th} is the thermal velocity of electrons, σ is the electronic capture cross section, n_i is the intrinsic carrier density, E_i is the intrinsic level of the semiconductor, and E_s is the energy level of the interface state. At 90°K, taking σ to be 10^{-15} cm^2 and v_{th} to be 10^7 cm/sec, τ_{en} is found to be 10 sec when the interface state is 0.21 eV below the conduction band. If the temperature is raised to 99°K, then the level of the interface state that has τ_{en} = 10 sec is at 0.24 eV below the conduction band. If we take one deep-depletion curve at 90°K and another at 99°K, then the voltage shift between the lower portions of the two curves represents the voltage drop across the oxide caused by the presence of electrons in those interface states which lie in the range from 0.21 eV to 0.24 eV below the conduction band. In this way the number of interface states with energy levels from 0.21 eV to 0.24 eV below the conduction band can be obtained. By raising the temperature still more, we can probe further into the bandgap in a similar way.

In Fig. 2.1, four sets of deep-depletion and light-assisted curves are shown for different temperatures on the same sample. The temperatures were 89°K, 122°K, 158°K and 204°K for curve sets 1, 2, 3 and 4 respectively. An important feature to observe in this figure is that as the temperature was increased, the height of the ledge in the light-assisted curve decreased. This was due to the increase of electron concentration at the SiO_2-Si interface when the temperature was raised, so that the current caused by the capturing of electrons into the holes in the

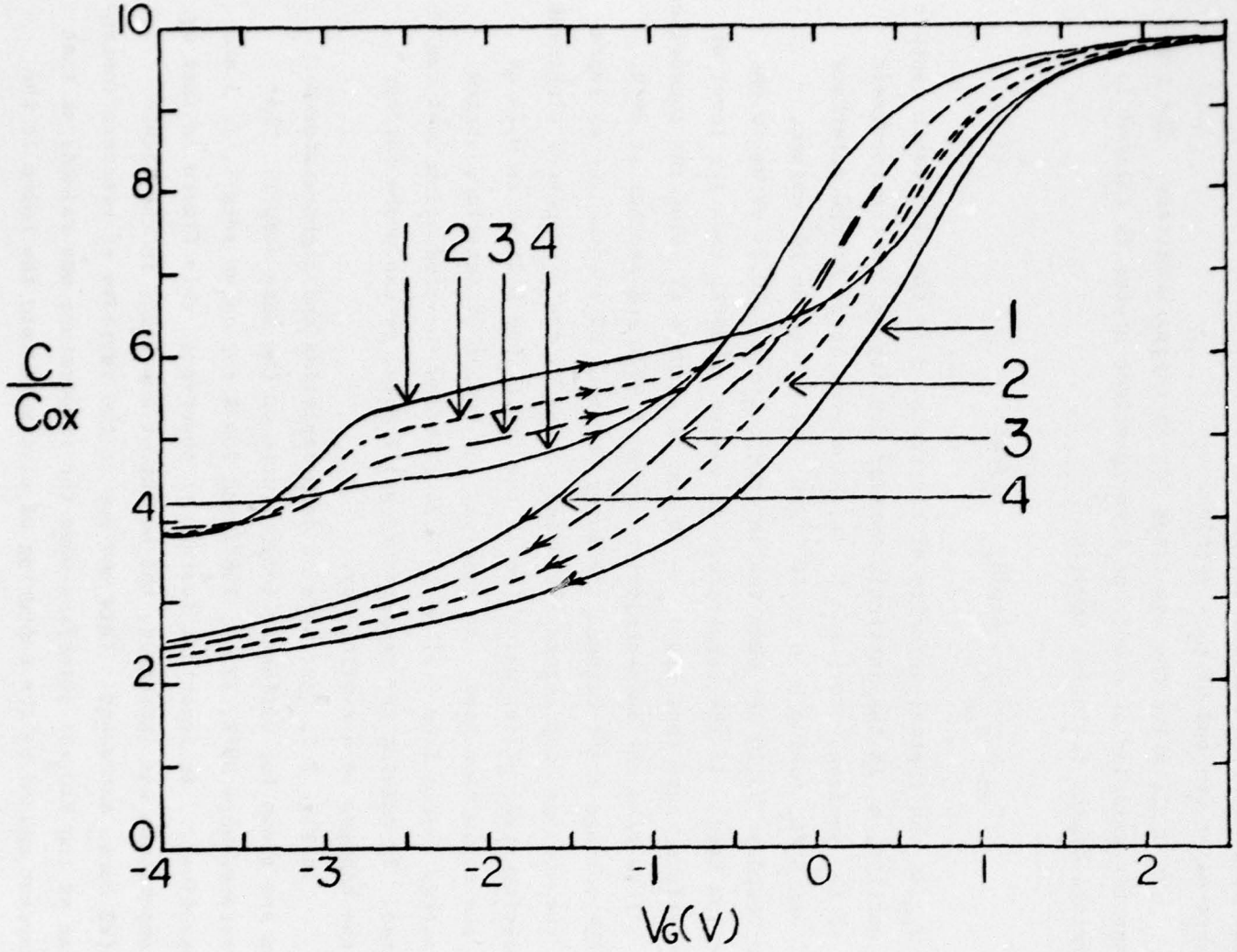


Fig. 2.1. Four sets of deep-depletion and light-assisted C-V curves taken at 89°K (Set 1), 122°K (Set 2), 158°K (Set 3) and 204°K (Set 4).

interface states began to dominate at a lower surface potential. The result of this reduction in ledge height is to reduce the length of the parallel portion of the light-assisted curve. As can be seen, this parallel portion is not present in the light-assisted curves 3 and 4 in Fig. 2.1. This fact prevents us from utilizing the parallel portions of the light-assisted curves to probe the interface-state distribution in the lower bandgap.

Table 2.1 shows an example of determining the interface-state distribution from the temperature-dependent voltage shift of the lower, parallel portion of the deep-depletion curves. The first column gives the sample temperature in °K. The second column shows the difference in energy between the conduction band edge and the level of the interface state which has an electron emission time constant τ_{en} of 10 sec. The value of $(E_c - E_s)$ is calculated from Eq. (2.1), which can be written as

$$E_c - E_s = \frac{E_g}{2} + kT \ln(\tau_{en} v_{th} \sigma n_i) \qquad (2.2)$$

For computation of the values given in the second column we have assumed $v_{th} = 10^7$ cm/sec and $\sigma = 10^{-15}$ cm^2. We also make the assumption, as we did in Sec. 3.2 of the last report,[1] that for those states which lie below the level where $\tau_{en} = 10$ sec the electrons will be frozen in the states during the period when the deep-depletion curve is taken, while for those states which lie above the level for which $\tau_{en} = 10$ sec the electrons will be emitted into the conduction band. The third column of Table 2.1 gives the difference in $E_c - E_s$ between consecutive temperatures. The fourth column gives the voltage shift in the lower parallel portion of the deep-depletion curves between two consecutive temperature settings. At 168°K, the interface-state level with $\tau_{en} = 10$ sec is 0.415 eV below the conduction band edge. This means that only the portion of the deep-depletion curve which has a normalized capacitance smaller than 0.45 will be parallel to the ideal deep-depletion curve. [Note: The Fermi level at 168°K is 0.11 eV below the conduction band edge, and the normalized capacitance is 0.45 when the surface potential is at -(0.415 - 0.11) = -0.305 eV.] Hence it is necessary to measure the voltage shift only in this very low portion of the deep-depletion curve.

T(°K)	$E_c - E_s$ (eV)	$\Delta(E_c - E_s)$ (eV)	ΔV(v)	ΔN_{ss} (cm^{-2})	n_{ss} ($cm^{-2}eV^{-1}$)
89	0.214	0.019	0.067	7.12×10^9	3.75×10^{11}
93	0.223	0.015	0.082	8.71	5.81
99	0.238	0.018	0.105	11.15	6.20
106	0.256	0.020	0.097	10.30	5.15
114	0.276	0.020	0.081	8.60	4.30
122	0.296	0.028	0.091	9.67	3.45
133	0.324	0.029	0.097	10.30	3.55
144	0.353	0.013	0.084	8.92	6.86
149	0.366	0.023	0.075	7.97	3.47
158	0.389	0.026	0.084	8.92	3.43
168	0.415				

Table 2.1. This table demonstrates the procedure for finding the interface state distribution by varying the sample temperature. See text for explanation.

In the fifth column, ΔN_{ss} is the number of interface states corresponding to the ΔV in the fourth column. The relation between ΔN_{ss} and ΔV is given by $\Delta N_{ss} = C_{ox} \Delta V/q$, where C_{ox} is the oxide capacitance per unit area and q is the electronic charge in coulombs.[1] In the sixth column, n_{ss} is the average interface state density obtained from the equation $n_s = \Delta N_{ss}/\Delta(E_c - E_s)$. The relation between n_{ss} and the corresponding energy level is shown by the horizontal bars in Fig. 2.2. The bars are connected by dotted lines to indicate roughly the distribution of interface states. Except for the high bar plotted above approximately 0.37 eV (for which we have no explanation), the bars show a reasonably smooth distribution of interface states. Also shown in Fig. 2.2 is the interface-state distribution (solid curve) calculated by Kuhn's method from a quasi-static C-V curve taken at 66°C.

Two major deviations of the dotted curve from the solid curve are: First, the dotted curve shows a reduction in interface state density near the band edge, while the solid curve shows a monotonic increase. It is difficult, at this point, to judge which determination is closer to the true interface-state distribution. Yeow et al[6] have done an error analysis on Kuhn's method of determining interface-state density. They show that toward the Si band edges, the interface-state distributions calculated by Kuhn's method are extremely sensitive to errors in the oxide capacitance measurement and in the determination of the integration constant. This causes the energy range of a valid measurement to be limited to approximately $\pm$ 0.3 eV above and below midgap, or to 0.26 eV away from both band edges. Since our first deviation occurs at energy levels which are smaller than 0.25 eV from the conduction band, it is in the range where Kuhn's method is not dependable.

It should be noticed that the peak in the dotted curve is not similar to the peak usually observed when the Gray-Brown method[4] is applied to measure the interface-state density near the band edges. The peak observed by the Gray-Brown method is usually within 0.15 eV from the band edges, and this peak could be ficticious as has been indicated by Boudry.[7] He conducted a computer-simulated Gray-Brown measurement using interface-state distributions and electron capture cross sections as measured by Deuling et al.[8] The result showed that although the assumed interface state distribution was monotonically increasing, the simulated Gray-Brown measurement showed a peak. The peak was due to a strong rolloff in the

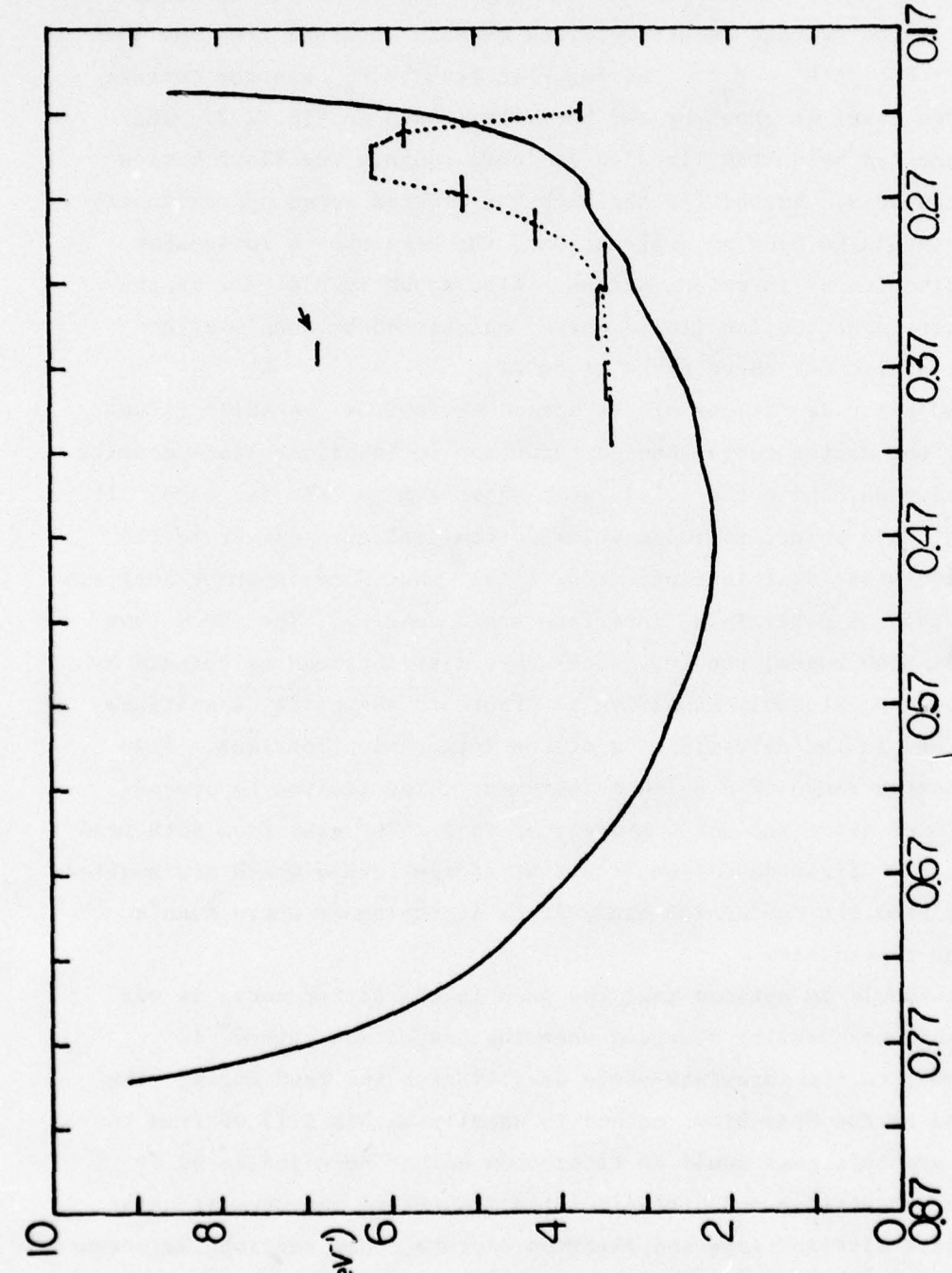


Fig. 2.2. Interface state density (cm^{-2} eV^{-1}) vs. energy level of the state as measured from the conduction band edge. Horizontal bars are obtained from Table 2.1. The solid curve is obtained by Kuhn's method.

electron capture cross sections near the band edge. With a measuring frequency of 150 kHz the interface states above the level where $E_c - E_s$ = 0.1 eV will not respond to the measuring signal, but those states which are below this level and are close to the Fermi level will respond to the measuring signal and contribute to the measured capacitance. This causes an error in determining the flatband voltage, which in turn produces a spurious peak in the interface-state distribution. In order to decrease the error to within 10%, a measuring frequency greater than 200 MHz is necessary. Hence, one can not reliably interpret the peak obtained by Gray-Brown measurements.

We shall now examine whether the roll-off in electron capture cross section has an effect on our method of measuring interface state density. In our method, we rely on the principle that at a particular temperature T_1, the emission time constants of electrons increase sharply as the levels of interface states lie deeper into the bandgap. This allows us to pick a interface-state level E_s where τ_{en} = 10 sec, and we assume that the electrons that are in the states below E_s will be forzen-in during the time when the deep-depletion curve is taken, while the electrons in the states above E_s will have time to be emitted into the conduction band. This assumption is certainly good as long as the electron capture cross section σ remains constant so that τ_{en} decreases monotonically toward the Si band edge. If σ has a sharp roll-off near the band edge, an examination is necessary to check the monotonicity of τ_{en}. The value of σ measured by Deuling et al[8] was approximately 10^{-15} cm^2 for states 0.20 eV away from the band edge, and the roll-off occurred for states that lay nearer the band edge. Boudry has indicated that σ can be approximated by the following equation:[7]

$$\sigma = 10^{-15} \{1 + \exp [(E_s - E_c + 0.16)/0.013]\}^{-1} cm^2 \qquad (2.3)$$

Since we are concerned only with the roll-off region where the exponential term is much larger than unity, we may approximate (2.3) by

$$\sigma = 10^{-15} \exp[(E_c - E_s - 0.16)/0.013] \ cm^2 \qquad (2.4)$$

Substituting Eq. (2.4) into Eq. (2.1), we have

$$\tau_{en} = \frac{1}{v_{th} n_i \sigma_o} \exp\left(12.3 - \frac{E_g}{2kT}\right) \cdot \exp\left[(E_c - E_s)\left(\frac{1}{kT} - \frac{1}{0.013}\right)\right]$$

where $\sigma_o = 10^{-15}$ cm^2 is the value of σ in the midgap region.

In order to have a monotonically decreasing τ_{en} towards the Si band edge, the requirement is

$$\frac{1}{kT} - \frac{1}{0.013} > 0$$

which provides the criterion

$$T < 151°K$$

Hence, as long as we conduct our measurements at temperatures less than 151°K we will not have to worry about the difficulties produced by the roll-off of σ.

The second deviation of the dotted curve from the solid curve in Fig. 2.2 is that the dotted curve has a consistently higher value than the solid curve when $(E_c - E_s)$ is larger than 0.25 eV. The reason for this deviation is not clear. Two possibilities occur to us: First, if the roll-off of σ is sharper than that of Eq. (2.3), then the basic assumption used in our method may become invalid at a threshold temperature less than 151°K. The consequence will be that the electrons in some states which are close to the band edge will not be emitted into the conduction band during the period of supposed emission. We would then obtain a reading of interface-state density higher than the true density. Secondly, it seems legitimate to wonder whether the number of interface states may be a function of temperature so that at lower temperatures one would see more interface states.

Finally, we shall say a few words concerning the difference between the Gray-Brown method and our own. With the Gray-Brown method,[4] the shift in flat-band voltage is used to measure the number of interface states (per cm^2) located in the energy range that is scanned by the Fermi level when the temperature is changed. In order to get a true reading of

the flatband voltage, a measuring frequency higher than 200 MHz is required to eliminate the interface-state capacitance at the flatband condition,[7] as was mentioned earlier in this section. When taking C-V curves, it is also necessary to use a ramp rate which is slow enough that the sample remains in equilibrium with the gate bias, at least until the flatband condition has been reached. With our method, the lower portion of the deep-depletion curve is utilized. The values of measuring frequency and ramp rate are not critical as long as the sample can be driven into the deep-depletion regime, and this is easily achieved at low temperature. With the Gray-Brown method, the effect of the roll-off of σ, as represented by Eq. (2.3), is to cause a spurious peak near 0.1 eV below the conduction band edge if the measuring frequency is within 150 KHz to 1.5 KHz. With our method, a roll-off would cause a misreading in interface state density when the energy range is more than 0.371 eV away from the conduction band edge. (Note: This level is where τ_{en} = 10 sec at 151°K.) And, lastly, by varying the temperature from 89°K to 151°K, the Gray-Brown method will cover the energy range from 0.056 to 0.113 eV below the conduction band. Our method will cover the range from 0.214 to 0.371 eV below the conduction band edge. Thus, the application of both methods will provide a wider coverage over the upper-half of the bandgap.

2.2(B) Some Possible Difficulties With the LTD Method

In order to apply the LTD method correctly it is necessary to be able to identify in the rising edge of the light-assisted curve a section whcih is parallel to the corresponding portion of the deep-depletion curve, i.e., the portion between points A and B of curve Set 2 in Fig. 2.3. The ledge height is reduced and the parallel portion vanishes if the sample temperature is too high, as was seen in Fig. 2.1. In the following, we shall describe three other cases where the LTD method can not be properly used.

Figure 2.3 shows two sets of 90°K C-V curves. Set 1 was taken after a sample had been high-field stressed at 90°K, brought up to room temperature and then cooled down to 90°K again. In the rising edge of the light-assisted curve of Set 1, there is an easily identifiable portion (A-B)

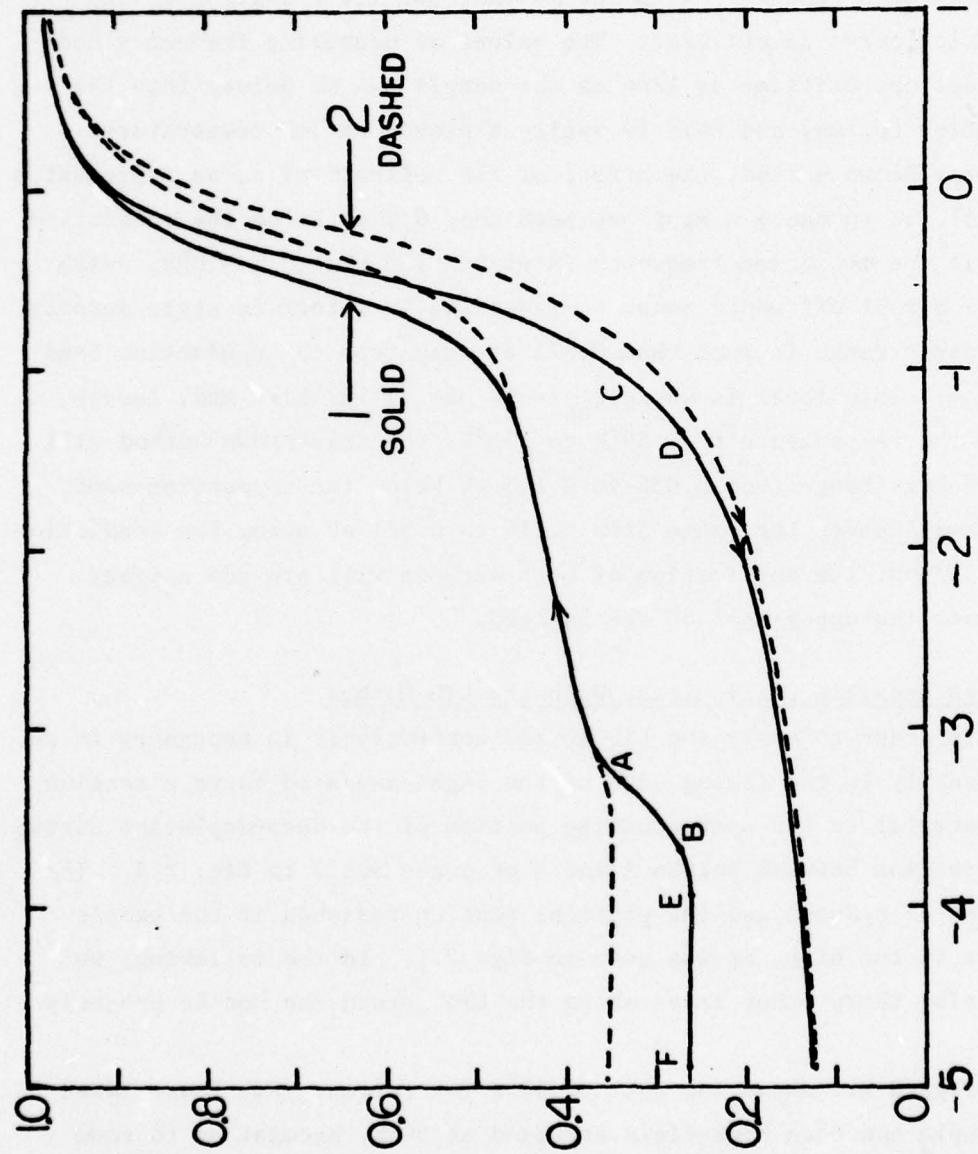


Fig. 2.3. 90°K C-V curves. Set 1: Taken after a sample was high-field stressed at 90°K, warmed up, and cooled down to 90°K again. Set 2: After the same sample had been held at room temperature for approximately 21 days.

which is parallel to the corresponding portion of the deep-depletion curve (C-D), and the LTD method can be applied without a problem. But if the sample was allowed to sit at room temperature for a sufficiently long time, the low-temperature light-assisted curve (between point E and F) began to rise and finally reached the level shown by the dashed curve (Curve 2). This curve has no identifiable parallel portion, and the LTD method can no longer be applied with accuracy. A possible explanation for the rising of the flat portion of the light-assisted curve could be an increase in the number of defects in the Si substrate near the $Si-SiO_2$ interface. These defects might trap holes so that before the gate voltage was ramped up to take the light-assisted curve, fewer free holes were available in the interface region. The interface potential would then be forced to increase (in the case of n-type sample) so that the hole current away from the interface could balance the external charging current. The increase in interface potential requires a decrease in the width of the depletion region. Consequently, the capacitance during this period would be raised.

Another difficulty in applying the LTD method can arise when lateral nonuniformities are present in the capacitor. These will not only distort the lower part of the deep-depletion curve from the ideal deep-depletion curve,[9,10] but will also prevent the occurrence of the parallel portions between the light-assisted and the deep-depletion curve. This can be easily seen by superimposing two sets of light-assisted and deep-depletion curves having relative displacements along the horizontal axis.

The third difficulty occurs when the capture cross sections of the interface states have markedly different values at different energy levels, as was discussed in some detail in the previous section. The consequence will be a distorted set of C-V curves similar to those caused by lateral nonuniformities.

2.3. Spatial Distribution of the High-Field-Generated Electron Traps

In this section we shall describe two approaches that we used to obtain information concerning the spatial distribution of the high-field-generated electron traps in the oxide.[1,2] First, we examined the thickness dependence of the C-V shift (caused by the charging of the traps). In the

second approach we examined the bias dependence of internally photoinjected current.

2.3(A) Thickness Dependence

Table 2.2 shows the amount of C-V voltage shift caused by charging of the high-field-generated traps. Here ΔV_1 is the voltage shift for the 1950Å oxide and ΔV_2 is the voltage shift for the 990-Å oxide. These data were obtained by adding the following two voltage shifts in the C-V curves: (1) The shift between the 90°K deep-depletion C-V curves of a sample before and after the high-field stress. This accounts for the charging of the electron traps by electrons which tunneled into the oxide during the stress. The trapping of holes which could have been generated by impact ionization is neglected because the field intensities used in obraining the data of Table 2.2 were not large enough to cause negative C-V shifts after high-field stress. (2) The voltage shift ΔV_{sat} caused by the charging of the electron traps by the internal photoinjection of electrons. The internal photoinjection was performed after the sample was warmed to 66°C for a period of time and cooled to 90°K (see Sec. 3.4(B) of the last report[1]).

ΔV_1 and ΔV_2 were measured after both oxides were stressed with the fields shown in Column 1 of Table 2.2 for a period of 30 min. The voltage shifts are shown in Columns 2 and 3, and Column 4 gives the ratio $\Delta V_1/\Delta V_2$. These results provide some insight concerning the spatial location of the generated traps. If the trap generation occurs only at the interface, then we may expect $\Delta V_1/\Delta V_2 = d_{ox1}/d_{ox2}$, for the total number of generated traps should, for the same stress field, be the same for both oxides. However, if the trap generation is a bulk effect so that the traps are generated uniformly throughout the oxide layer, then we may expect $\Delta V_1/\Delta V_2 = (d_{ox1}/d_{ox2})^2$, for in this case the total amount of traps generated and the distance to the charge centroid are both proportional to the thickness. The results shown in Col. 4 of Table 2.2 support the view that the trap generation is a bulk phenomenon, for which would expect $\Delta V_1/\Delta V_2 = (d_{ox1}/d_{ox2})^2 = 3.9$.

E (MV/cm)	ΔV_1 (v)	ΔV_2 (v)	$\Delta V_1/\Delta V_2$
7.1	0.69	0.23	3.0
7.2	0.84	0.20	4.2
	0.99		4.9
7.3	1.41	0.37	3.8
7.4	1.68	0.38	4.4

Notes: 1. ΔV_1 — d_{ox1} = 1950 Å (d_{ox1}/d_{ox2}) = 2.0

ΔV_2 — d_{ox2} = 990 Å $(d_{0x1}/d_{ox2})^2$ = 3.9

2. Stress Temperature = 90°K

Stress Time = 30 min

Table 2.2. Dependence of electron-trap generation on the oxide thickness. Here E is the stress field (same on both 990Å and 1950Å oxides) applied at 90°K, ΔV_1 is the voltage shift of the deep-depletion curve caused by charging of the generated traps for the 1950 Å oxides, and ΔV_2 is the corresponding voltage shift for the 990 Å oxides.

2.3(B) Internal Photoemission Experiment

The photoinjection I-V characteristics can be analyzed to extract information about the charge distribution in the oxide layer of an MOS capacitor.[11,12] This technique is applied in the present section.

A 1950Å sample with an initial flatband voltage of -1.2V was high-field stressed at 90°K with a field of 7.5 MV/cm for 60 min. Following the stress, and while the sample was still maintained at 90°K, 1.47×10^{13} cm^{-2} of electrons were photoinjected into the oxide by 5 eV light. This caused the deep-depletion C-V curve to shift in the positive direction by approximately 4.75 V, showing net negative oxide charging. With the 5 eV light still illuminating the sample, the substrate current vs. gate voltage were measured point-by-point as the gate voltage was varied from +10V to -7.5V. The results are plotted in Fig. 2.4. Following the photo I-V measurement, a set of 90°K C-V curves were taken which showed almost no change from the curves taken before the photo I-V measurement, showing that the space charge had not been perturbed by the measurement.

From Powell and Berglund's[11] analysis, if there is only negative charge residing in the oxide, and if there is no charge located in the image-force potential well, we may expect to have almost zero current when the gate voltage lies between two voltages, designated as V_- and V_+ in Fig. 2.4, which are obtained by extrapolating the two principal portions of the I-V curve to zero current. We find larger currents in the region between V_- and V_+ than would be expected from the simple model. This could be due to the presence of charge in the image-force potential well adjacent to the injecting contact,[11] or it could be due to a lateral nonuniformity in the sample.[11] By comparing the measured deep-depletion C-V curves before and after high-field stress, we observed that a slight lateral nonuniformity had been introduced into the sample by the stress, and that this non-uniformity was preserved after the subsequent internal photoinjection. Hence both of the aforementioned causes may be responsible for the tailing that we observe between V_- and V_+ in Fig. 2.4. The shape of the tailing in the gate-positive regime is different from that of the gate-negative regime.

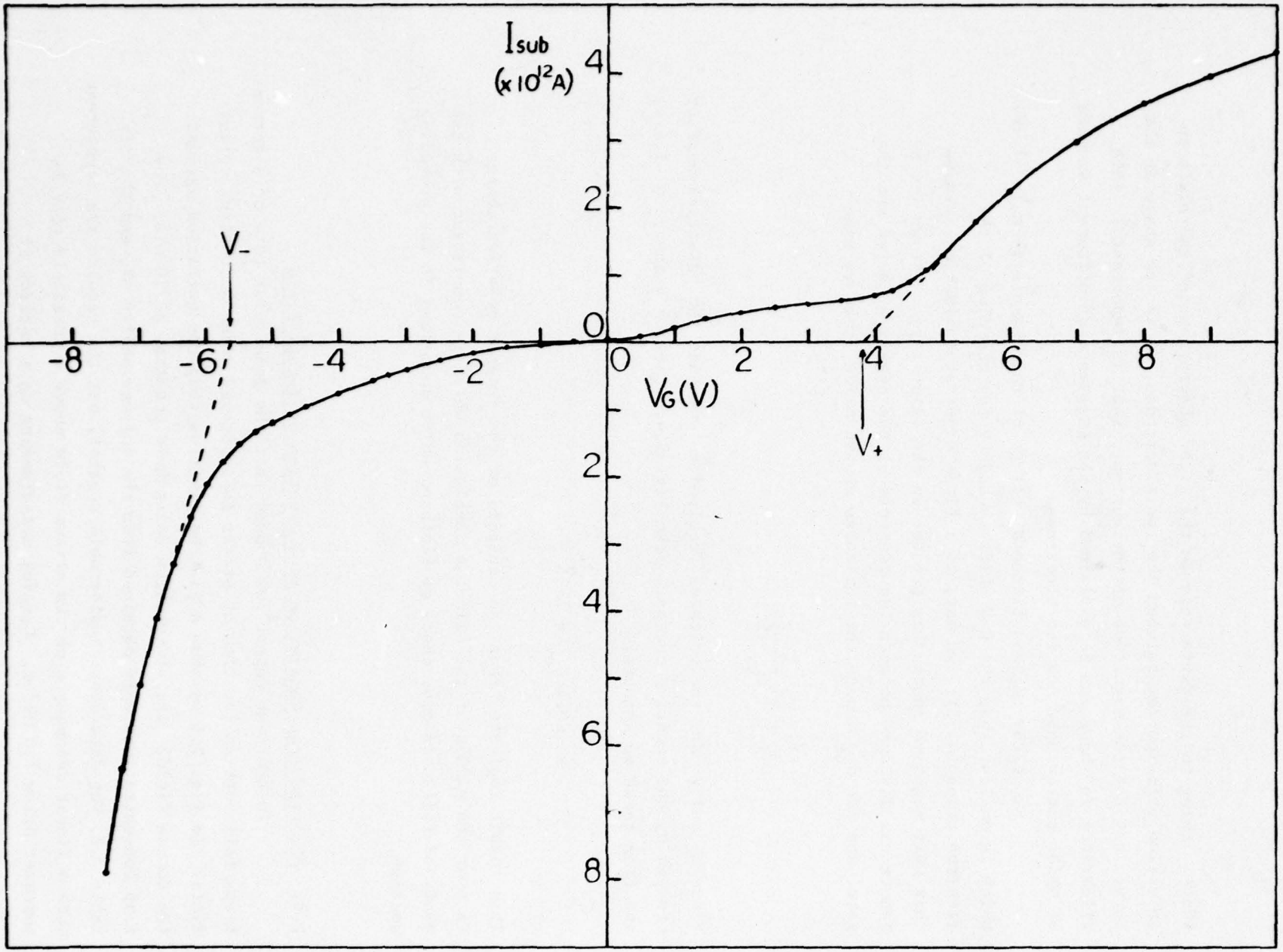


Fig. 2.4. Photoinjection V-I curve taken after an RCA 1950 Å oxide was stressed at 90°K with a field of 7.5 MV/cm for 1 hr, followed by photoinjection of 1.47×10^{13} cm^{-2} electrons into the oxide.

(Note: Owing to the difference in the light absorption and the electron injection efficiencies between the two electrodes, it is the shape of the curve, but not the magnitude of the current, that is important.) This difference in shape can be explained by the existence of different amounts of oxide charge near the two electrodes.

Since the initial flatband voltage of this sample is only -1.2V, which is smaller than the C-V shift caused by the charging of the electron traps (4.75V), we may, to a first order approximation, assume that only negative charge was present in the oxide layer. If we let $\bar{x}$ denote the distance between the centroid of the negative charge and the gate, and let d_{ox} denote the thickness of the oxide, then we have

$$\frac{V_+}{|V_-|} = \frac{\bar{x}}{d_{ox} - \bar{x}}$$

since V_+ and V_- are the voltages required to overcome the potential barrier created by the negative charge. From Fig. 2.4, $V_+ = 3.8$ V and $V_- = -5.6$ V, and from these we compute:

$$\bar{x} \approx 0.4\, d_{ox} = 780\text{Å}$$

This result indicates that the centroid of the trapped negative charge is near the middle of the oxide, a conclusion which is consistent with the observed thickness dependence of flatband shift described in the preceding section.

2.4. Electron Trap Generation as a Function of Stress Field

In the last report[1] we showed that the generation rate of electron traps falls off as the time of stress is increased under a constant stress field. In Fig. 2.5 we show a plot of electron trap concentration against the stress field, the stress time being held constant at 30 min. The trap concentrations were obtained from the voltage shifts ΔV_1 and ΔV_2 of Table 2.2. The data show considerable scatter, but the results are consistent with a linear dependence on the stress field above a threshold that is somehwat below 7.0 MV/cm. Careful measurements on a variety of

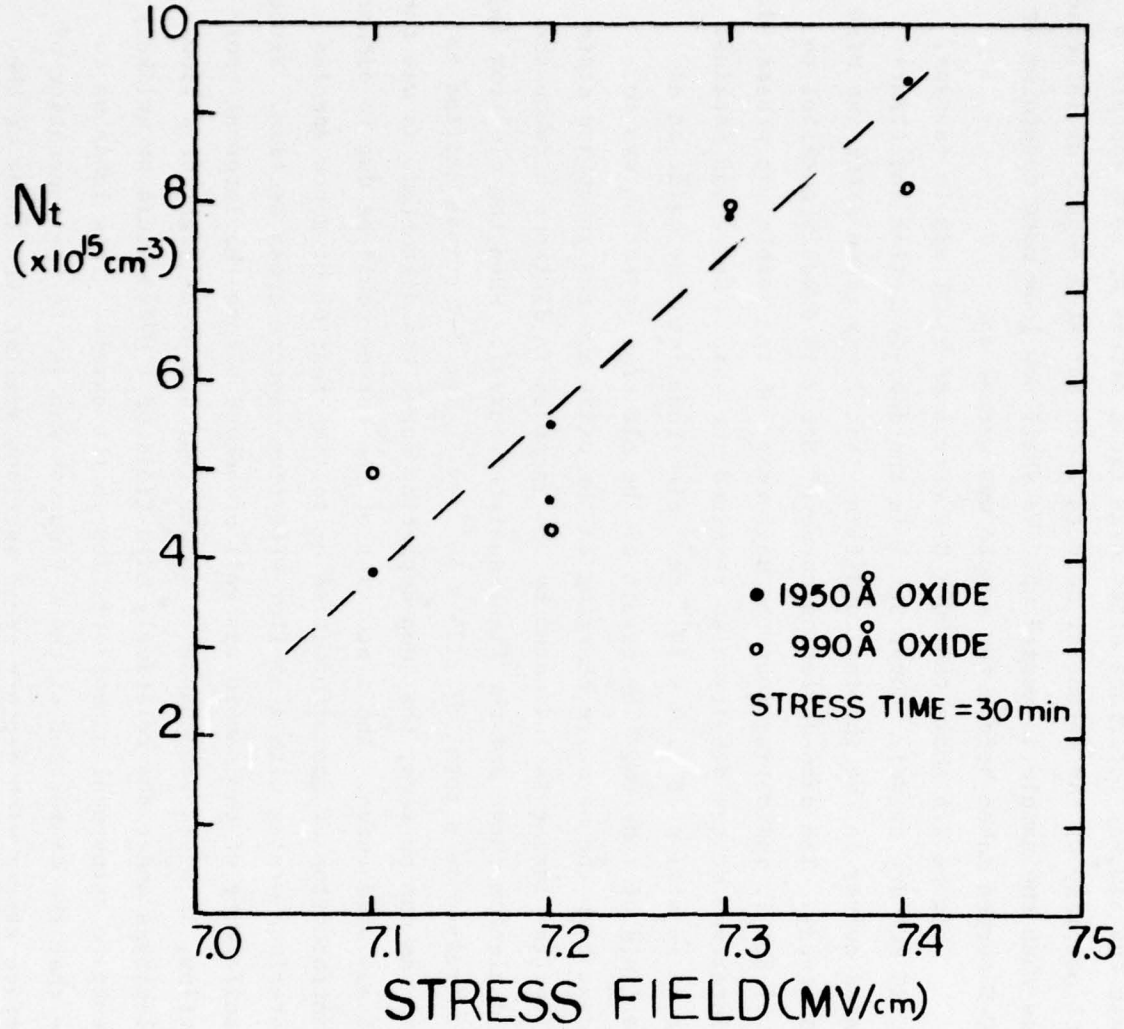


Fig. 2.5. Concentration of electron traps generated by high-field stress as a function of stress field for both the 1950 Å and 990 Å oxides. The stress time was 30 min.

samples indicate a threshold of approximately 6.8 MV/cm.

2.5. On the Donor-Like Interface States Introduced by Internal Photoinjection at 90°K.

In the last report[1] we mentioned that the injection of electrons through the SiO_2-Si interface after high field stress at 90°K appears to anneal out many of the potential defects which act as a source of interface states when the sample is warmed up. We shall now look more carefully at the C-V curves taken before the sample was warmed up.

Figure 2.6 shows the 90°K C-V curves of a BTL sample (n-type, 920Å, 3% HCl dry oxide). Curve Set 1 is the deep-depletion and light-assisted curves in the initial condition. Set 2 was taken after the high field stress. The deep-depletion curve of Set 2 is exactly parallel to that of Set 1, indicating that the uniformity of the sample was preserved. The interface states density also remained the same. Set 2 was obtained after an injection of 1.14×10^{14} cm^{-2} electrons into the oxide at an oxide field of 1 MV/cm. The result of the electron injection was to increase both the negative charging in the oxide and the interface state density (the latter is indicated by the increase in distance between the deep-depletion curve and the light-assisted curve). When the electron injection was increased to a total of 2.79×10^{14} cm^{-2}, the C-V curves shifted to Set 4. As can be seen, the deep-depletion curve was distorted, as was the light-assisted curve. The distortion of the curves could be due to either the introduction of nonuniformities or to the creation of a new species of interface states with a smaller effective capture cross section. Since the uniformity of the sample was well preserved before the internal photoinjection, it seems reasonable to assume that 4.8 eV UV light or a flow of electrons under the relatively mild field of 1 MV/cm would be unlikely to generate structural nonuniformities in the sample. This leads us to argue that the distortion of the C-V curves was due to the generation of interface states with capture cross sections smaller than those of the original interface states. From the facts that the lower part of the deep-depletion is parallel to the initial deep-depletion curve and that the distortion occurs in an abrupt kink, it seems clear that the capture cross

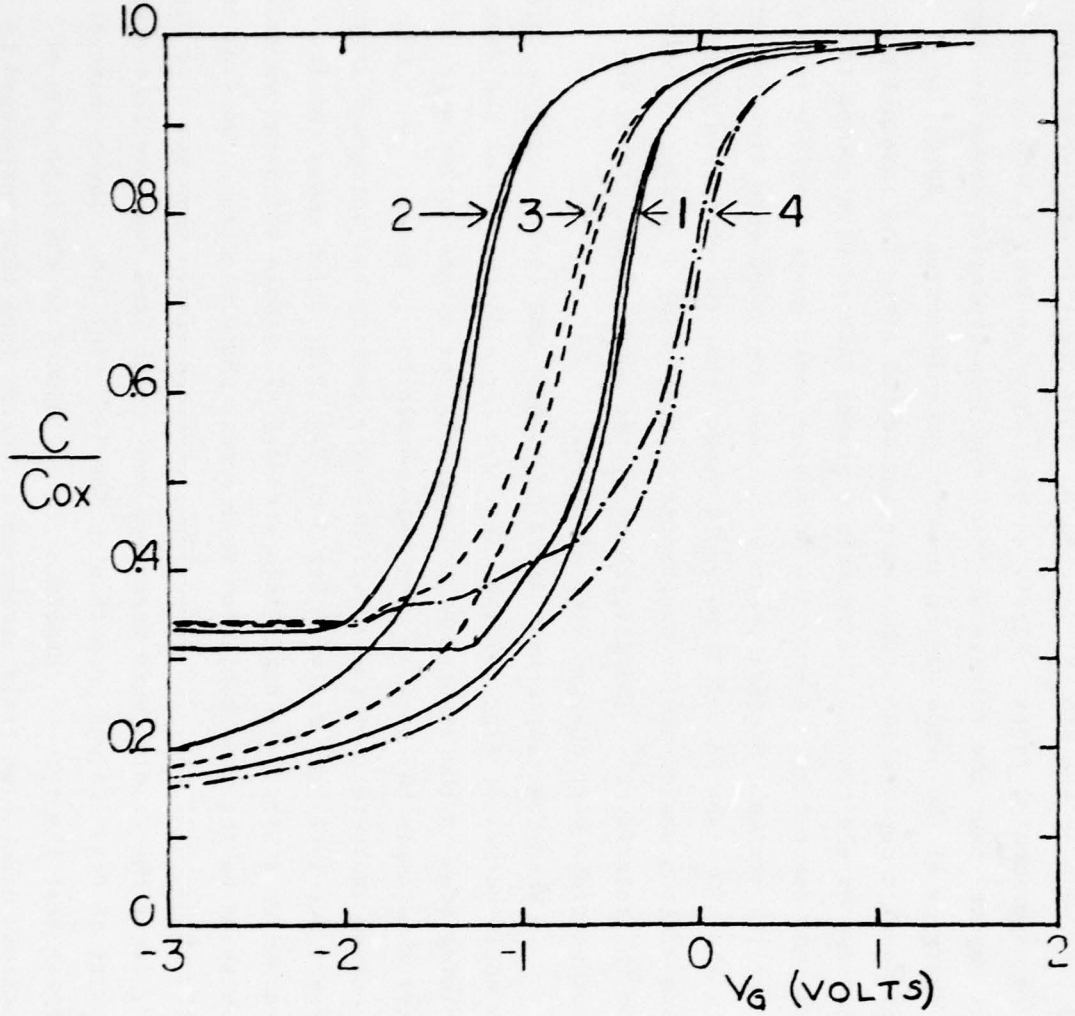


Fig. 2.6. 90°K deep-depletion and light-assisted C-V curves for a BTL sample. Set 1: Initial condition. Set 2: After high-field stress at 90°K with 7.4 MV/cm for 30 min. Set 3: After 1.82 x 10^{-5} C/cm^2 of electrons were injected into the SiO_2 from Si by internal photoinjection. Set 4: After additional electron injection to a total dose of 4.47 x 10^{-5} C/cm^2.

section of the new interface states was either of a single value or of some distributed set of values with a sharp cut-off at the lower end. The origin of these states could be the coulombic potential of the trapped electrons in the electron traps which were generated by high field stress and located near the SiO_2-Si interface. This model is consistent with three experimental facts: First, we have shown in Sec. 3.3(C) of the last report[1] that the voltage shift of the deep-depletion curve was caused by charging of the oxide during internal photoinjection. Hence, no additional acceptor-like states were introduced after the internal photo-injection of electrons. The interface states induced by electron-injection were thus donor-like. A negative potential could quite possibly induce donor-like states. Secondly, since the electron traps were distributed into the SiO_2 (see Sec. 2.3) we would expect that the effective capture cross section would have an exponentially decreasing dependence on distance from the interface.[13] Thirdly, these states appeared only after the electron traps were charged with electrons.

When the sample was warmed up to 66°C and cooled down, we obtained the solid curves of Fig. 2.7 (see Sec. 2.2 for a discussion of the lack of a rising edge in the light-assisted curve). The dashed curves were obtained after the sample had been at room temperature for 10 hours. Both sets of curves indicate that the interface-state density had decreased greatly. Compare Set 1 of Fig. 2.6 with Set 3 of Fig. 2.8, which shows results obtained on a similarly high-field stressed BTL sample which was warmed up without having been subjected to internal photoinjection. We find that although Set 4 of Fig. 2.6 shows more interface states than Set 2 of Fig. 2.8, after the samples were warmed up and cooled down the interface-state density of Fig. 2.6 was less than in Set 3 of Fig. 2.8. These observations suggest that the type of interface states induced by the injection of electrons after high field stress is different from that introduced by the high-field stress alone. The latter can be annealed by the electron injection, while the former was induced by electron injection and are reduced in number after warm-up.

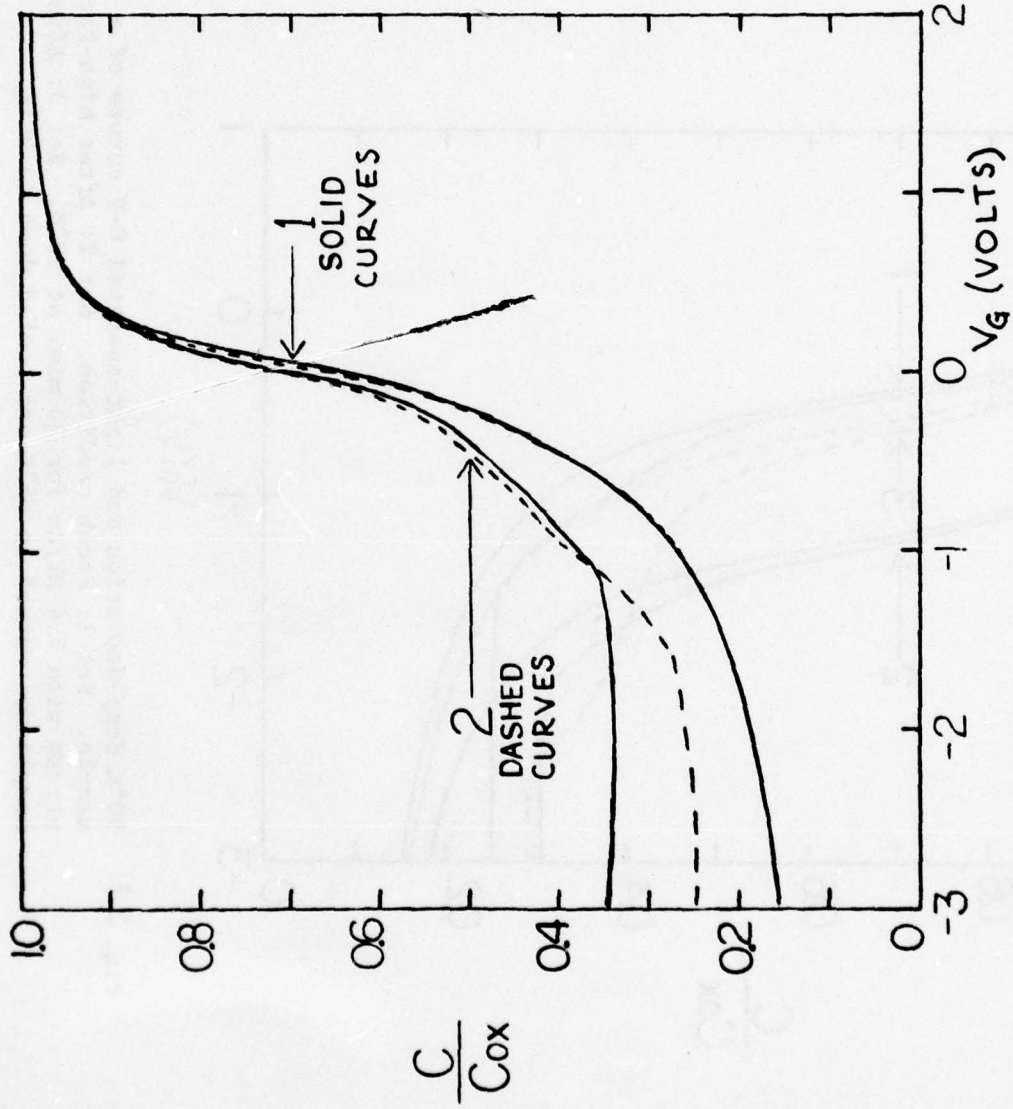


Fig. 2.7. Continuation of Fig. 2.6. Set 1: Taken after the sample was warmed up to 66°C and cooled down to 90°K. Set 2: Taken after the sample had been at room temperature for 13 hours.

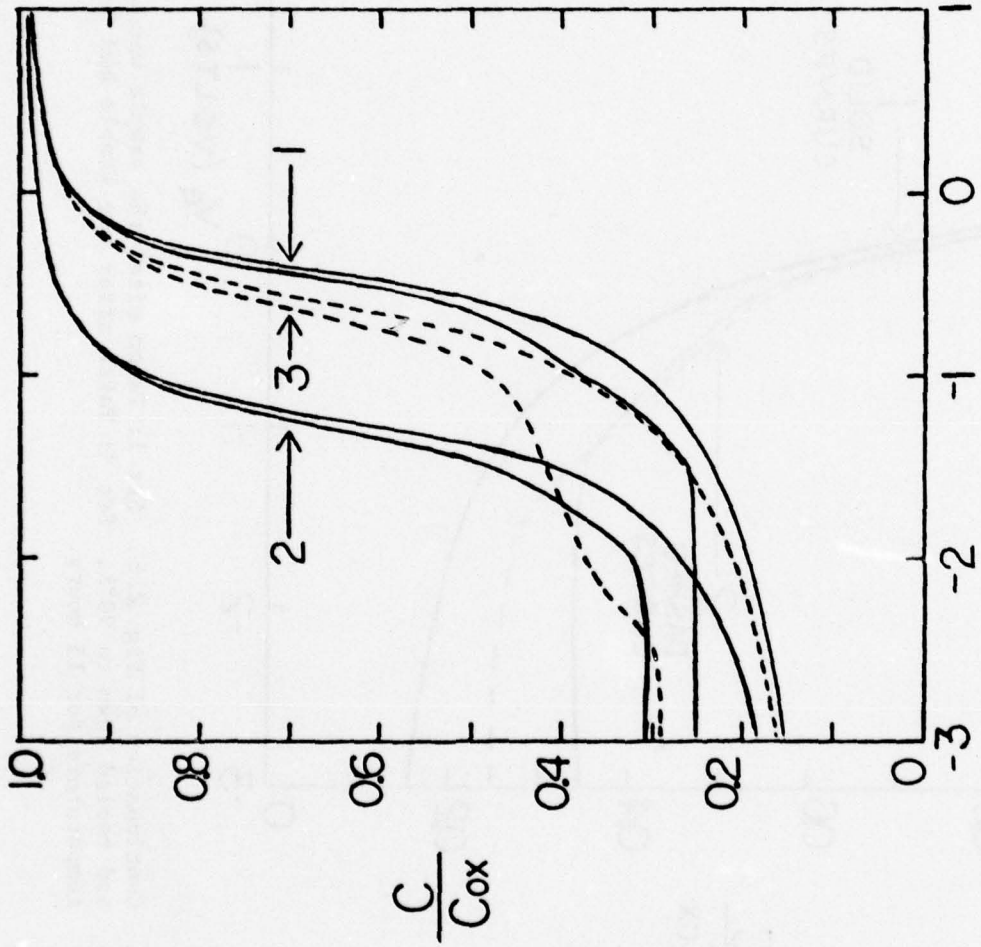


Fig. 2.8. 90°K deep-depletion and light-assisted C-V curves of a BTL sample. Set 1: Fresh condition. Set 2: After high-field stress with 7.4 MV/cm for 30 min. at 90°K. Set 3: After the sample was warmed to 65°C and cooled down to 90°K.

In HCl-steam grown RCA samples, similar effects were observed. However, the kinks in the deep-depletion and light-assisted curves were almost negligible.

Finally, a phenomenon related to the interface-state generation induced by internal photoinjection will now be described. The phenomenon will be demonstrated with the aid of Table 2.3. The samples were RCA 1950Å wet oxides on n-type substrates. The portion of the table which is above the dashed line is duplicated from Table II on p. 35 of the last report.[1] The samples and the stress conditions were the same for the data of both tables. Our interest here is the amount of interface states, N_{ss}, as measured by the LTD method, after electrons were injected into the oxide. With sample 4201, electrons were injected at 90°K with an injection field of 1 MV/cm. After injection, N_{ss} increased from 3.43×10^{11} to 4.06×10^{11} cm^{-2}, or $\Delta N_{ss} = 0.63 \times 10^{11}$ cm^{-2}. The sample was then warmed up, and N_{ss} began to decrease as was described previously. In the last step of Table 2.3, N_{ss} of sample 4201 was reduced to 3.46×10^{11} cm^{-2}, which is very close to the value before the electron injection, i.e., 3.43×10^{11} cm^{-2}. For sample 4200, the electron injection was instead performed at 66°C, but with the same injection field and the same amount of total injection charge as that of sample 4201. After injection, N_{ss} changed from 3.36×10^{11} cm^{-2} to 4.19×10^{11} cm^{-2} more than the corresponding N_{ss} sample of 4201. This difference can be explained by the fact that, as already mentioned in Section 4.3, the interface-state generation of a high-field stressed sample can be increased by applying a moderate field at 55°C but not at 90°K. During the period of internal photoinjection of sample 4200, a field of 1 MV/cm was applied for approximately 3 hours in total. In the 4th line for sample 4201 in Table 2.3, it is seen that the application of a field of 1 MV/cm, without the simultaneous injection of electrons, increased N_{ss} by 0.21×10^{11} cm^{-2} in 3 hours. This value is very close to the difference, 0.20×10^{11} cm^{-2}, in ΔN_{ss} between samples 4200 and 4201 after they had electron photoinjection at 66°C and 90°K respectively. Hence, it is plausible to assume that of the increase in N_{ss} of sample 4200 after electron injection (0.83×10^{11} cm^{-2}), one part was due to the increase of interface states induced by electron injection (0.63×10^{11} cm^{-2} from comparison with sample 4201) and the

Sample No. 4200			Sample No. 4201		
	N_{ss} (cm^{-2})	ΔN_{ss} (cm^{-2})		N_{ss} (cm^{-2})	ΔN_{ss} (cm^{-2})
Initial.....	2.38×10^{11}		Initial.....	2.28×10^{11}	
		0.89×10^{11}			0.85×10^{11}
After high-field stress			After high-field stress		
1st warmup.....	3.27×10^{11}		1st warmup.....	3.13×10^{11}	
		0.09×10^{11}			0.05×10^{11}
33 hr at 25°C..... (E_{bias} = 0 V/cm)	3.36×10^{11}		4 hr at 55°C..... (E_{bias} = 0 V/cm)	3.18×10^{11}	
					0.21×10^{11}
			3 hr at 55°C..... (E_{bias} = 1 MV/cm)	3.39×10^{11}	
. . . . .			. . . . .		
		0.83×10^{11}			0.01×10^{11}
e-inj at 66°C..... (E_{bias} = 1 MV/cm)	4.19×10^{11}		13 hr at 25°C.... (E_{bias} = 0 V/cm)	3.40×10^{11}	
		0.07×10^{11}			0.03×10^{11}
19 hr at 25°C..... (E_{bias} = 0 V/cm)	4.26×10^{11}		1 hr at 55°C..... (E_{bias} = 1 MV/cm)	3.43×10^{11}	
		0			0.63×10^{11}
25 hr at 25°C..... (E_{bias} = 0 V/cm)	4.26×10^{11}		e-inj at 90°K.... (E_{bias} = 1 MV/cm)	4.06×10^{11}	
					-0.21×10^{11}
			18 min at 66°C... (E_{bias} = 0 V/cm)	3.85×10^{11}	
					-0.24×10^{11}
			30 min at 66°C... (E_{bias} = 0 V/cm)	3.61×10^{11}	
					-0.15×10^{11}
			20 hr at 25°C.... (E_{bias} = 0 V/cm)	3.46×10^{11}	

Table 2.3. N_{ss} obtained by the LTD method for two RCA samples subjected to the same high-field stress but with different warm-up conditions and different temperature for internal photoinjection. The part of the Table which is above the dashed line was shown in Table II, p.35, of the last report.[1]

other part was due to the interface-state enhancement by the application of the moderate field of 1 MV/cm at 66°C to the sample (0.20×10^{11} cm^{-2}, as suggested from the corresponding result obtained on sample 4201).

2.6 Summary

We have described a method for measuring interface-state distributions by varying the temperature of the sample. The energy range covered by this method is different from that of the Gray-Brown method[4] within the same range of temperature. Hence, the application of both methods will achieve a wider coverage of the interface-state distribution. We also discussed some of the difficulties that can cause difficulties in the application of the LTD method.

From the thickness dependence of the C-V voltage shift and also from the bias dependence of photocurrent, we find evidence that the high-field generation of electron traps is a bulk effect. With a stress field of 7.1 MV/cm to 7.4 MV/cm applied for 30 min, the resulting concentration of traps was in the range 10^{15} - 10^{16} cm^{-3}, and this concentration increased almost linearly as a function of stress field above a threshold field of 6.8 - 6.9 MV/cm.

Lastly, we showed that although the injection of electrons into the SiO_2 at 90°K after high-field stress increases the number of donor-like interface states, the number of these states was greatly reduced after the sample was warmed. However, if the electron injection was performed at 66°C, the interface states induced by the injection did not diminish in number. These facts will, we hope, provide additional clues concerning the atomic mechanisms responsible for the formation of interface states.

3. FURTHER INVESTIGATION OF RADIATION-INDUCED INTERFACE-STATE FORMATION IN MOS CAPACITORS

(J. J. Clement collaborating)

3.1. Introduction

The investigation of the influence of holes and the effects of temperature on the generation of new interface states in MOS capacitors exposed to ionizing radiation, which was first described in the last report,[1] has been continued. Results of experiments using a second set of MOS capacitor samples having an oxide layer thermally grown in dry oxygen are included in this report. These are also compared to the previously reported experimental results on samples with oxides thermally grown in HCl-steam.

In the last report[1] we presented evidence that irradiation of an MOS capacitor with soft X-rays at 87°K produces negligibly small change in the number of interface states if the capacitor is kept cold. However, an increase in interface states is observed when the sample is subsequently warmed. This increase occurs even if the holes are annihilated by recombination with photoinjected electrons before the warm-up process is begun. This indicates that only a temporary presence of the holes at the SiO_2/Si interface is required to initiate the interface-state generation process. The results of our most recent experiments using dry-grown oxides confirm these results previously obtained using the samples with steam-grown oxide. However, a study of the temperature dependence of the interface state generation process indicates some definite differences between these two types of samples.

3.2. Description of Samples

The MOS capacitors used in these later experiments were fabricated at Bell Telephone Laboratories through the courtesy of Dr. E. N. Fuls and Mr. E. LaBate. The substrate was n-type (100) silicon with 5-10 ohm-cm resistivity. On this wafer the gate oxide was thermally grown in a mixture of dry oxygen plus 3% HCl at a temperature of 1000°C to a nominal thickness of 1200 Å. This was followed by a 30-minute anneal at 1000°C in argon. The back contact was

formed by making an n^+ diffusion, and aluminum was then vacuum deposited on the back of the wafer. This was sintered in hydrogen for 30 minutes at 450°C. Semitransparent[14] (15Ω/□) circular aluminum field plates, approximately 30 mils in diameter, were then evaporated onto the front oxide surface. This set of MOS capacitors was designated BTL-51677.

The processing steps involved in the fabrication of the MOS capacitor samples with the steam-grown oxide used in previous experiments were described in our last report.[1] Those samples, designated RCA-72876C, were made for us at RCA Laboratories through the courtesy of Dr. K. M. Schlesier. The gate oxides of these samples were a radiation-hardened type developed at RCA.[15]

The main points in the preparation of these two sets of samples are summarized in Table 3.1. The BTL samples had a much smaller number of initial interface states than did the RCA samples. Hence, changes in the interface state concentration had a greater effect on the characteristics of the BTL samples which made the changes easier to detect.

The sample chamber and experimental apparatus were described in our last report.[1]

3.3. Measurements of Interface State Densities

Three methods for measuring interface states were used in these experiments. The technique utilizing the quasistatic C-V curve to determine the interface state distribution as described by Castagne[16] and Kuhn[17] was employed at a temperature of 333°K (60°C). The quasistatic and high-frequency C-V curves were recorded at this temperature because of the extremely long minority-carrier response time in the silicon substrates of our samples. The slight warming of the sample allowed us to use a reasonable ramping rate of 30 to 40 mV/sec which minimized the effects of leakage current and noise on the quasistatic curve.

At 87°K, a measure of the concentration of interface states across the central region of the silicon energy bandgap was obtained by using the ledge phenomenon observed in the high frequency C-V curves of MOS capacitors at low temperatures. An example of this

TABLE 3.1

DESCRIPTION OF TEST SAMPLES

Sample	RCA 72876C*	BTL 51677
Substrate	n-type, (100) silicon 5–10 Ω-cm resistivity	n-type, (100) silicon 5–10 Ω-cm resistivity
Gate oxide	Steam-HCl ambient at 875°C to a thickness of ∿1000 Å	Dry oxygen + 3% HCl at 1000°C to a thickness of ∿1200 Å
Post-oxidation anneal	10 min. at 950°C in nitrogen	30 min. at 1000°C in argon
Back contact	n^+ diffusion; evaporated aluminum	n^+ diffusion; evaporated aluminum sintered for 30 min. at 450°C in hydrogen
Field plate†	Semi-transparent aluminum (20 Ω/□) ∿40 mil diameter	Semi-transparent aluminum (15 Ω/□) ∿30 mil diameter

* Reference 15

† Reference 14

effect for a typical fresh RCA sample at 87°K is shown in Figure 3.1. Several investigators have observed this ledge phenomenon before and have correctly attributed this effect to the presence of interface states.[18-20] C. S. Jenq has recently given a more rigorous explanation of this effect and has shown what information about interface states can be obtained.[1] We originally termed this method the low-temperature ledge (LTL) technique, but we now designate it by the more descriptive name "low-temperature C-V displacement" (LTD). The main points of the LTD method were discussed in the last report.[1]

The width of the ledge, ΔV_{ledge}, as shown in Figure 3.1 can be used to determine the number of interface states in the central portion of the bandgap according to the formula:

$$N_i = C_o \Delta V_{ledge}/q \ (cm^{-2}) \qquad (3.1)$$

where C_o is the oxide capacitance per cm^2 and q is the magnitude of the electronic charge. As discussed in the last report,[1] the central region of the bandgap which includes those interface states responsible for the ledge phenomenon is approximately 0.7 eV wide at 87°K. Hence one can obtain an average concentration of interface states (in cm^{-2} eV^{-1}) for this region by dividing N_i (cm^{-2}) by 0.7 eV.

The Gray-Brown shift of the flat band voltage as the sample is cooled from 333°K to 87°K provides another means of measuring the number of interface states present in the upper part of the band gap.[21,22]

These three techniques complement each other, and, in addition, they serve to check each other in their regions of overlap.

3.4. Influence of Holes and Temperature on Interface State Formation

Previous investigations into the process of interface-state formation in MOS devices exposed to ionizing radiation have shown that the direct interaction of radiation at the $Si-SiO_2$ interface is not needed in order to produce interface states; however, interface-state formation is dependent on the transport of radiation-produced holes to the interface.[23,24] In one study, it was determined that the major

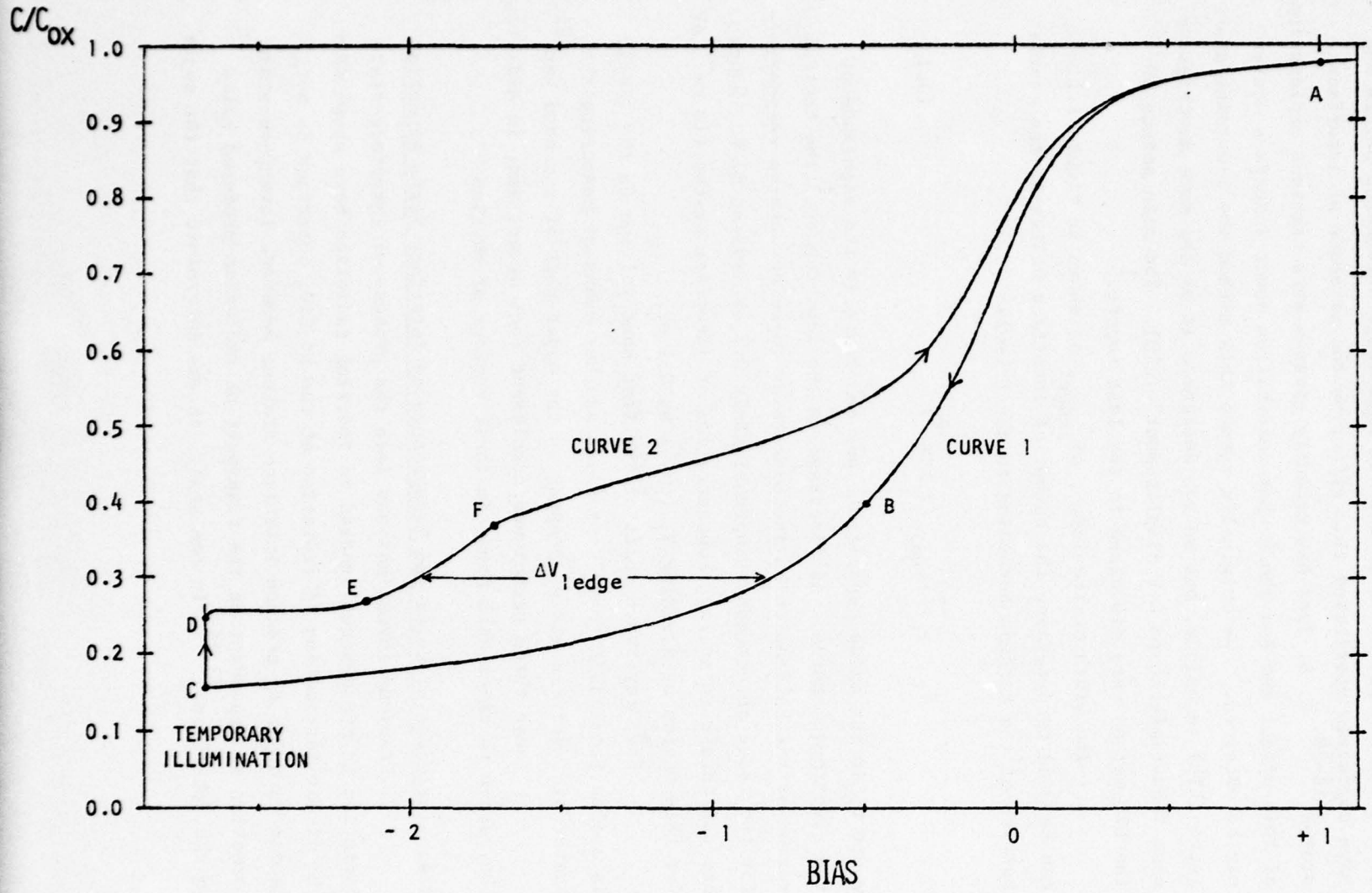


Fig. 3.1. Example of the low-temperature-ledge effect in C-V curves of a fresh RCA 72876C sample at 87°K.

part of the interface state generation occurs after the holes have had time to reach the interface.[25]

It is well established that holes in thermally grown silicon dioxide are subject to a temperature-activated, field-dependent transport process through the oxide.[26-33] Thus, at liquid nitrogen temperatures and for low values of applied electric field, the holes are essentially immobile and are trapped through the oxide near the point of creation. However, it has been shown that the motion of holes through the oxide can be enhanced by applying higher electric fields and/or by illuminating the device with light having photon energies in the range from 1.6 to 2.0 eV.[33,34]

The purpose of these experiments was to further examine the connection between the transport of radiation-produced holes to the SiO_2/Si interface and the creation of interface states, as well as the effect of temperature on the interface-state formation process. The general experimental procedure used in the study of the dry-oxide BTL samples was the same as that used on the wet-oxide RCA samples described in the last report.[1] To review briefly: After recording the initial high-frequency and quasistatic C-V curves at 333°K, the MOS capacitor sample was cooled to 87°K, and the initial interface state density was measured by the LTD method. The sample was then exposed to soft X-rays to produce hole-electron pairs; the electrons were rapidly swept out by a low electric field applied to the sample during irradiation, leaving the holes trapped through the oxide. The holes could then be transported to one interface or the other by applying a larger electric field together with excitation by visible light. The remaining holes were annihilated by recombination with photoinjected electrons.[35,36] The interface state density was again measured by the LTD method, and the sample was then warmed to observe possible temperature effects on interface state generation. The results of these experiments on the BTL samples are summarized in Table 3.2 as follows:

Column I identifies the sample. A fresh sample was used each time. All fresh samples were essentially identical.

Column II shows the number of interface states, N_i (cm^{-2}), as determined on the fresh sample at 87°K by the LTD method, using Eq. (3.1).

I SAMPLE	II N_i (CM^{-2}) INITIAL	III V_G DURING IRRADIATION	IV V_G BIAS FOR 3 HR.	V N_i (CM^{-2}) BEFORE WARM-UP	VI N_i (CM^{-2}) AFTER WARM-UP	VII ΔN_i (CM^{-2}) (COL. VI - COL. II)
BTL-1	1.4×10^{10}	NO X-RAY	+ 36 V	1.4×10^{10}	1.4×10^{10}	0.0×10^{10}
BTL-2	1.9×10^{10}	+ 18 V	NO BIAS TREATMENT	2.2×10^{10}	7.3×10^{10}	5.4×10^{10}
BTL-3	2.4×10^{10}	- 18 V	- 36 V	2.4×10^{10}	6.4×10^{10}	4.0×10^{10}
BTL-4	2.4×10^{10}	+ 18 V	+ 36 V	$\lesssim 3.4 \times 10^{10}$	14.9×10^{10}	12.5×10^{10}

Table 3.2

Study of interface state generation using BTL 51677 samples. See text for explanation.

Column III shows the applied gate voltage during a 20-minute irradiation with soft X-rays at 87°K. This bias will quickly drift the radiation-produced electrons to the positive electrode but will result in very little transport of holes in the oxide at this temperature. Since the soft X-rays will penetrate to the SiO_2/Si interface, some holes will be produced and trapped in this critical interfacial region. Also, it appears that holes generated in the bulk of the SiO_2 will have some initial motion before being immobilized in traps,[26,27] and with a positive gate bias, this motion will bring some holes into the interface. With a negative gate bias, some of the radiation-produced holes in the substrate may drift into the interfacial region. Thus, we expect some trapping of holes near the interface for either polarity of gate voltage, but, at these low fields and without light assistance, the main body of the holes in the bulk of the oxide will be essentially immobile at 87°K.

Column IV lists the gate bias which was applied for three hours at 87°K to transport the radiation-produced holes through the bulk of the oxide. The transport of holes during this period was assisted by illuminating the sample with visible light[33,34] which was provided by a Bausch and Lomb tungsten-halide lamp source filtered through a water cell and a yellow (3-68 Corning) filter. After the drift of the holes through the oxide, any remaining holes, whether trapped in the bulk or at the interface, were annihilated by recombination with photoinjected electrons at 87°K. Ultraviolet light with a photon energy of approximately 5 eV was used for this purpose.

Column V gives the density of interface states at 87°K after the treatment just described. Comparison with Column I shows that the number of interface states remains essentially unchanged at 87°K after the exposure of the sample to X-rays, transport of holes through the oxide, and photoinjection of electrons to annihilate the remaining holes.

Column VI shows the effect of warming the sample. The sample was kept at room temperature for several (approximately 12-18) hours. The high-frequency and quasistatic curve was shallower and broader (with

the exception of sample BTL-1) than the intial curve indicating an increase in interface states. The sample was again cooled to 87°K so that a direct comparison of N_i could be made using the LTD technique. As indicated by the larger values of N_i listed in this column, the width of the low temperature ledge had increased. In addition, the Gray-Brown shift of the flatband voltage was larger than it was for the fresh sample. All three tests indicate that interface states were generated upon warming of the sample.

Column VII shows the net increase in interface states that resulted from variations in experimental treatment of the four samples.

We can make the following observations from the results shown in Table 3.2. First, from Column V, we see that none of the sequences resulted in an appreciable increase in interface states so long as the sample was held at 87°K. The interface states appeared only during or after warmup. Second, the four different sequences show appreciable differences in Column VII as follows: On Sample BTL-1, which had no X-irradiation and served as a control sample, the increase in N_i after warming was negligible. On Sample BTL-2, which was irradiated with positive gate bias but which had no subsequent drift of holes to either interface, the increase in interface states was a moderate one which may be associated with holes that were produced near the interface and trapped there. On Sample BTL-3, where the holes produced in the oxide bulk were transported to the gate, the increase in interface states was similarly moderate in value. The slight difference between Samples BTL-2 and BTL-3 is most likely due to the decreasing interface field as the positive charge build-up occurs during irradiation for the case of negative gate bias. On Sample BTL-4, however, where the holes in the bulk were transported to the SiO_2/Si interface, the increase in interface states is quite appreciably greater. These results are quite similar to those observed in the experiments using the RCA samples as was described in the last report.[1]

Thus, the generation of interface states appears to be associated with holes at the interface, and nearly all the states make their appearance after the sample is warmed. However, since

the holes were annihilated by recombination before the sample was warmed, merely the temporary presence of holes at the interface appears to be sufficient to start the interface-state generation process. This behavior suggests that the formation of interface states is not a purely electronic process but is electrochemical in nature, perhaps involving bond breaking and relaxation of borken bonds.

3.5. Temperature Dependence of the Interface-State Formation Process

In order to obtain more information on the temperature dependence of the interface state generation process, the following experiment was performed. Sample BTL-4, having undergone the treatment outlined in Sec. 3.4 and Table 3.2, was warmed in a series of increasingly larger heating and cooling steps much like those described for an RCA sample in the last report.[1] Following the annihilation of the remaining radiation-induced holes by recombination with photo-injected electrons, the sample was warmed to a particular temperature and kept there for one hour. It was then cooled to 87°K to measure the change in the interface state density using the LTD method. The sample was heated (and cooled to 87°K) in successive steps to temperatures of 110, 130, 160, 190, 220, 250, 290, 333°K. The total increase in the number of interface states following the final heating step was 1.25×10^{11} cm^{-2} as computed from the net change in the width of low temperature ledge. The percentage of this increase, which was observed following each step of the heating and cooling cycle, is shown in Figure 3.2. Uncertainty in the exact percentage of the increase in the number of interface states below 190°K is indicated in this figure (by the +'s and x's connected with a line). This uncertainty was a result of a double bump in the light-assisted curve for this sample which, of course, affects the measurement of the low temperature ledge used to determine the concentration of interface states. This effect was not observed on the fresh sample, and shrank as the sample was warmed, vanishing completely with the sample was warmed to 190°K. This was the only sample for which this effect was detected. A likely explanation for this observation is the presence of positive ions on

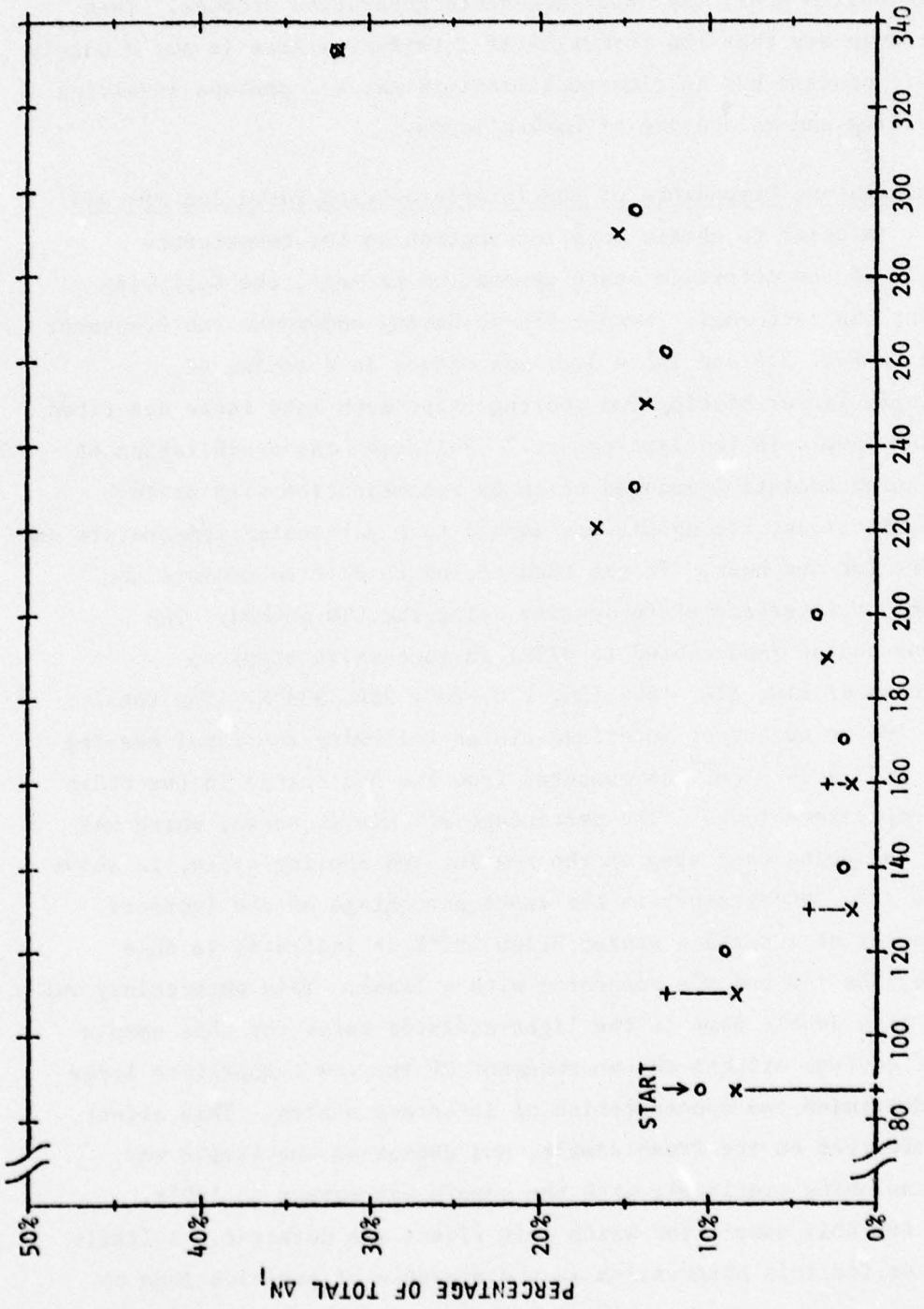


Fig. 3.2. Effect of temperature on the generation of new interface states in BTL MOS capacitors irradiated at 87°K.

x - + Sample BTL-4; total $\Delta N_1 = 1.25 \times 10^{11}$ cm^{-2}.

o Sample BTL-6; total $\Delta N_1 = 9.7 \times 10^{10}$ cm^{-2}.

the sample surface around the field plate which could create a small reservoir of electrons when the sample is biased into deep depletion. After the temporary illumination of the sample, in the course of ramping the applied bias up toward accumulation, at a certain surface potential it would be possible for these electrons to fill some of the interface states giving rise to the two bumps observed only in the light assisted curve. As the sample was warmed, then, the ions may have been removed from the surface.

In order to help resolve this uncertainty another sample (BTL-6) was subjected to a similar experimental treatment. The sample was cooled to 87°K, and the initial concentration of interface states was measured via the LTD technique. With the gate biased at +18 V, it was exposed to soft X-rays for 22 minutes. The sample, with the temperature still at 87°K, was then biased at +36 V for three hours while illuminated with visible light from the Bausch and Lomb tungsten-halide lamp filtered through a water cell and a yellow (3-68 Corning) filter. As described previously, this procedure transports the radiation-produced holes trapped throughout the oxide bulk to the SiO_2/Si interface. Electrons were photoinjected into the oxide to recombine with the remaining holes, and the interface state concentration was again determined using the LTD method.

The sample was next warmed to a particular temperature and held there for one hour, then cooled to 87°K so that any change in the number of interface states, as detected in the low temperature ledge, might be noted. The sample was heated (and cooled to 87°K) in successive steps to temperatures of 120, 140, 170, 200, 230, 262, 295, 333°K. The total increase in the number of interface states following the last heating step was 9.7×10^{10} cm^{-2}. The percentage of this increase which was observed following each step of the heating and cooling cycle is shown by the circles (o's) in Figure 3.2.

It is apparent from comparing the x's and o's in this figure that the interface state generation in these two samples closely follows the same general trend.

Sample BTL-4 was kept at room temperature for 7 days and the concentration of interface states was once again checked using the LTL technique. The interface states had increased by less than 0.35×10^{10} cm^{-2}, which is a change of about 2.7% of the total. Therefore, one can conclude that essentially all of the interface states are generated within one hour of warming the sample.

The results of a similar experiment performed on an RCA MOS capacitor sample with a steam-grown oxide, which was described in the last report,[1] is reproduced here in Figure 3.3. Comparing the results in Figures 3.2 and 3.3, the obvious difference between the two types of samples is that the BTL dry-grown oxide has a smaller percentage of interface states generated below 190°K than did the RCA steam-grown oxide. The difference is made up in the temperature range between 220 to 290°K, the last heating step (to 333°K) having about the same percentage of interface states generated for both samples.

The task of drawing conclusions from the information in Figures 3.2 and 3.3 is made difficult by the lack of an adequate general theory on the origin and physical nature of interface states.[37] This type of experiment might be useful in studying the effects of impurities, such as water or hydrogen, introduced during oxide growth, post-oxidation anneals, or other variations in processing parameters on the temperature dependence of the radiation-induced interface-state parameters. If a controlled study of this type were carried out, one might be able to obtain some insight concerning the true nature of the radiation-induced interface states. For example, the interface states generated in the heating steps below 190°K in the experiments described above could possibly be associated with the presence of hydrogen or water (OH) at the interface and the breaking of Si-H or Si-OH bonds, since one might expect the RCA steam-HCl grown oxides to have more of these bonds at the interface than the BTL dry oxygen-HCl grown oxides. This is purely conjecture at this point, however. More work in this area is indicated.

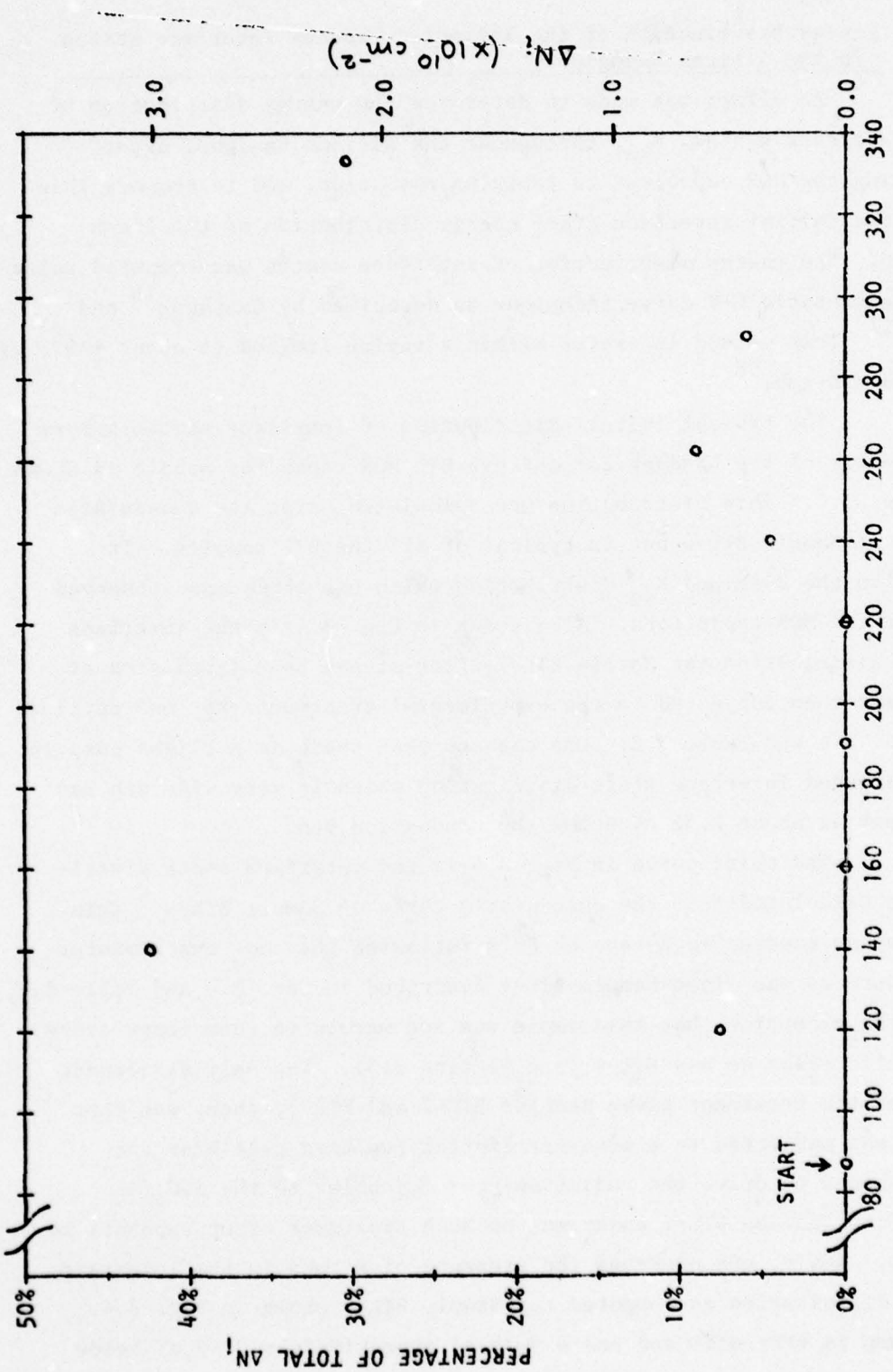


Fig. 3.3. Effect of temperature on the generation of new interface states in an RCA MOS capacitor irradiated at 87°K. Total $\Delta N_1 = 7.1 \times 10^{10}$ cm^{-2}. (Taken from Fig.2.2 of Ref. 1.)

3.6. Energy Distribution of the Radiation-Induced Interface States in the Silicon Bandgap

An effort was made to determine the energy distribution of the interface states, N_{ss}, throughout the silicon bandgap, after exposing the MOS capacitor to ionizing radiation, and to compare this with the initial interface state energy distribution of the fresh sample. The energy distribution of interface states was computed using the quasistatic C-V curve technique as described by Castagne[16] and Kuhn.[17] This method is useful within a region limited to about $\pm$ 0.3 eV around mid-gap.[38]

The typical initial distribution of interface states across the center of the bandgap for a fresh BTL MOS capacitor sample is shown in Fig. 3.4. This distribution was calculated using the quasistatic curve of Sample BTL-2 but is typical of all the BTL samples. It exhibits the U-shaped N_{ss} distribution which has often been observed before the MOS capacitors. Also shown in Fig. 3.4 is the interface state distribution for Sample BTL-2 after it had been irradiated at 87°K and then subjected to the experimental treatment that was outlined in Sec. 3.4 and Table 3.2. One can see that there is a slight bump in the computed interface state distribution which is very wide and has its peak at about 0.52 eV below the conduction band.

The third curve in Fig. 3.4 is the interface state distribution calculated from the quasistatic curve of Sample BTL-5. This sample was exposed to X-rays at 87°K following the same experimental procedure as was given Sample BTL-4 described in Sec. 3.4 and Table 3.2, with the exception that this sample was not warmed to room temperature in cyclic steps as was BTL-4 (see Section 3.5). The only difference between the treatment given Samples BTL-2 and BTL-5, then, was that BTL-5 was subjected to a post-irradiation positive gate bias for three hours to drive the radiation-produced holes to the SiO_2/Si interface whereas BTL-2 underwent no such treatment after exposure to X-rays. Again, one observes the presence of a bump in the interface state distribution as computed for Sample BTL-5 shown in Fig. 3.4. The bump is very wide and has a peak at approximately 0.49 eV below

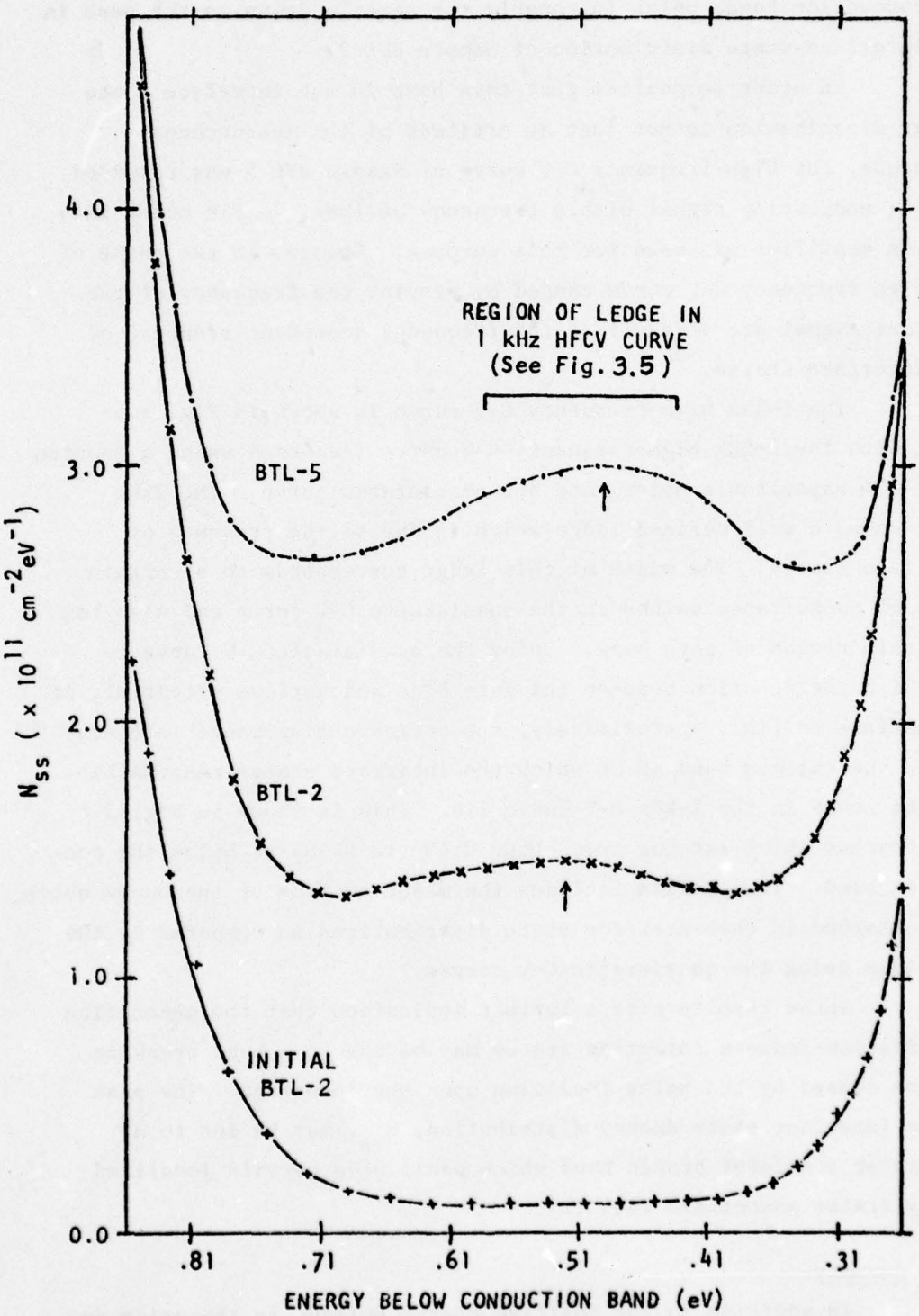


Fig. 3.4. Energy distribution of radiation-induced interface states in BTL MOS capacitor samples as determined from quasi-static C-V curves.

the conduction band, which is roughly the same location as the peak in the interface-state distribution of Sample BTL-2.

In order to confirm that this bump in the interface state energy distribution is not just an artifact of the measurement technique, the high-frequency C-V curve of Sample BTL-5 was recorded using a modulating signal with a frequency of 1kHz. A PAR model 124A lock-on amplifier was used for this purpose. Changes in the shape of the high frequency C-V curve caused by varying the frequency of the a-c test signal are a result of the frequency dependent response of the interface states.[39]

The 1-kHz high-frequency C-V curve is shown in Fig. 3.5 along with the 1-MHz high-frequency C-V curve (recorded using a Boonton Model 72A capacitance meter) and the quasistatic curve. The 1-kHz curve shows a well defined ledge which is due to the presence of interface states. The width of this ledge corresponds to a certain range of capacitance values on the quasistatic C-V curve and also to a certain region of gate bias. Using the quasistatic C-V curve to establish the relation between the gate bias and surface potential, it is possible to find, approximately, the corresponding range in energy within the silicon bandgap at which the interface states responsible for the ledge in the 1-kHz C-V curve lie. This is shown in Fig. 3.4 by a bracket which extends from about 0.435 to 0.585 eV below the conduction band. This region includes the major portion of the bumps which were observed in the interface state distributions as computed by the technique using the quasistatic C-V curves.

These results give a further indication that the generation of radiation-induced interface states may be due to a bond breaking process caused by the holes impinging upon the interface. The peak in the interface state energy distribution, N_{ss}, may be due to a particular species of broken bond which would have certain localized energy states associated with it.

3.7. Summary

In addition to the positive charge buildup in the oxide due to the trapping of holes, another effect observed in MOS devices exposed

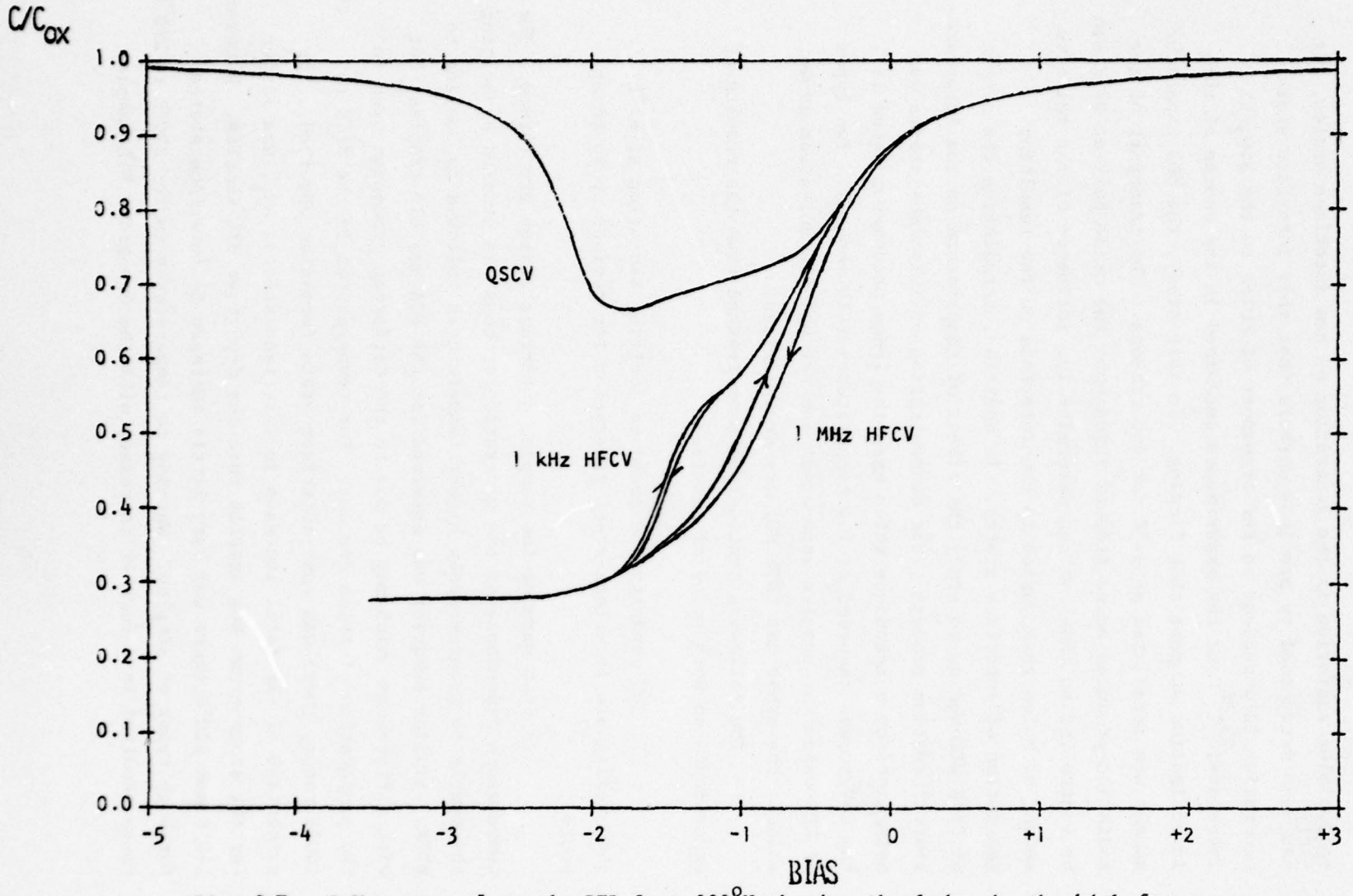


Fig. 3.5. C-V curves of sample BTL-5 at 333°K showing the ledge in the high frequency curve which appears by changing the frequency of the a-c test signal.

to ionizing radiation is the generation of new interface states. It has been determined by previous workers that this interface state generation is dependent on the transport of holes to the SiO_2/Si interface,[23,24] and the experiments performed in the course of this investigation support this finding. In this study, the MOS capacitor sample was irradiated at 87°K for two reasons. The transport of the radiation-produced holes trapped throughout the oxide bulk at 87°K can be controlled so that one can determine the influence of the relative amount of holes transported to the interface on the resulting generation of interface states. In addition, irradiating the sample at 87°K allowed us to study the effect of temperature on the interface-state formation process. The concentration of interface states was determined by a technique which uses the ledge phenomenon found in the C-V curves recorded at low temperatures (LTD method). Two types of MOS capacitor samples were used: one set had RCA HCl-steam grown oxides, the other had BTL HCl-dry grown oxides.

The following conclusions were reached from the results of experiments on both types of samples:

1) MOS capacitors exposed to ionizing radiation at 87°K show negligible interface-state generation for periods up to three hours.

2) Upon warming the sample, interface states are formed. The temperature dependence of the generation process was studied by heating the sample to progressively higher temperatures followed by cooling to 87°K. Similar behavior was observed for the RCA and BTL samples, but with differences which may be due to the different processes used in the preparation of these devices. For temperatures in the 87°K to 140°K range, there was some interface state formation observed. The percentage of the total increase in interface states, ΔN_i, was larger for the steam-grown RCA samples than the dry-grown BTL samples. Between 140°K and 220°K there was very little increase in interface states for both types of samples. Warming to temperatures in the 220°K to 290°K range resulted in a further increase, with the dry-grown BTL samples

showing a larger percentage increase of the total ΔN_i than the steam-grown RCA samples. The final heating step to 333°K showed a similar increase in the percentage of the total ΔN_i for both types of samples.

This type of experiment might be used in a controlled study of MOS capacitors in which variations in the preparation of the samples on the temperature dependence of the interface-state generation could be investigated. In this way, one might be able to determine the physical nature of the interface states and/or the mechanism of interface-state generation.

3) The interface-state generation takes place despite the fact that the holes had been annihilated by recombination with photoinjected electrons before the warm-up process was begun. However, at least the temporary presence of the holes at the SiO_2/Si interface was necessary to initiate the interface-state formation process.

For the BTL samples the energy distribution of the radiation-induced interface states, N_{ss}, was determined from the quasistatic C-V curve. A broad bump in this distribution was found which had its peak in the region between 0.435 and 0.585 eV below the conduction band. That this peak in N_{ss} was not an artifact of the measurement technique was confirmed by the appearance of a ledge in the high-frequency C-V curve when the frequency of the a-c test signal was lowered from 1 MHz to 1 kHz.

From the characteristics of the interface state formation observed in these experiments, it appears that the generation process is electrochemical in nature. More work is needed to determine the mechanism by which new interface states are created; however, it seems likely that one or more bond breaking processes are involved.

4. HIGH FIELD EFFECTS IN Al_2O_3 ON Si

(S. S. Li collaborating)

4.1. Introduction

The injection and conduction mechanisms of the charge carriers in Al_2O_3 films on silicon substrates have been investigated by many workers.[40-42] The very high concentration of the electron traps ($> 10^{18}$ cm^{-3})[1] whose spatial and energy distributions are quite complicated[43-46] causes these studies to be very difficult. However, it is believed that owing to the high electron trap density, trap-assisted tunneling is the major mechanism for the charge injection.[40-43]

Comparison of the current levels under high-field stressing at both room temperature and 100°K shows that temperature has a pronounced effect on the dark current. We also noted that a significant amount of charge which cannot be tunnel-emitted at high field and 100°K, and whose optical energy is deeper than 2.8 eV, can be thermally detrapped at low fields when the sample is warmed up to room temperature. Since the trap density is very high (average intertrap distance smaller than 75 Å), this indicates that thermally activated hopping between the traps contributes to bulk conduction in the Al_2O_3.

Self-quenched breakdowns were observed when gold field plates were used on the Al_2O_3-Si sutructure and when the insulator was biased to high fields with the field plate negative. The breakdown rate was found to increase with time. No self-healing breakdowns were observed with aluminum field plates, but destructive spots did appear on the gate. We also found the breakdown strength at 100°K is higher than at room temperature. Previously, we reported that the electrical-optical phonon scattering mean free path in the oxide appears to be 4-5 Å.[1,47,48] This indicates that impact ionization is not likely to contribute to the breakdown mechanism. We are studying this matter further.

4.2. Sample Description

The MOS capacitors, which were fabricated at Bell Laboratories by courtesy of David Boulin, had 90°C pyrolytic-grown Al_2O_3 on either

n-type or p-type (100) silicon with resistivity of 8-12 Ω-cm. Both gold and aluminum gates were evaporated on the oxide. The samples with aluminum gates had an oxide thickness of about 450 Å. The oxides with gold gates had different thicknesses, all in the 500 Å range.

4.3. Current Injection and Transport Mechanisms in the Thin Al_2O_3 Films

4.3(A). Room Temperature Measurements

The solid curves of Figs. 4.1(a) and 4.1(b) show the current versus time (from 10 sec. up to 10^4 sec.) for Al-Al_2O_3-Si structures subjected to different field stress at room temperature. The MOS dots used in these experiments were on the same wafer and located adjacent to each other. The current was observed to decay with time following the relation of $I \sim t^{-a}$, ($a = 0.38 - 0.75$), which was found by Walden.[41] The build-up of the charge storage in the film is shown in Figs. 4.2(a) and 4.2(b). We have reported previously[1] that the concentration of electron traps is larger than 10^{18} cm^{-3} and, to a first-order approximation, the capture cross section is $2 - 3 \times 10^{-13}$ cm^2. It seems likely that with this high trap density, trap-assisted tunneling may be the major injection mechanism for the Al_2O_3 film.[40-43] Trap-assisted tunneling depends on the interface field as well as on the spatial and energy distribution of the vacant traps available for tunneling.[49] The electron-trap spatial and energy distributions were studied by Harari and Royce[43,44] and by Noble Johnson.[45] They found that the energy levels extend from 2 eV down to deep levels. In our field-injected samples we also observe a significant amount of electron trappings distributed between 3 eV to 4 eV which corresponds to the C-band found by Harari and Royce.[43,44] Also, deep electron trapping appears to be very important in contributing to the flatband voltage.

Because of the large trap cross section, the charge build-up rate is very fast initially. This charge storage in the oxide reduces the interface field as well as the number of traps available for tunneling; therefore, decaying current is expected. The current is observed to keep on decaying for 50 hrs. without reaching a steady state.

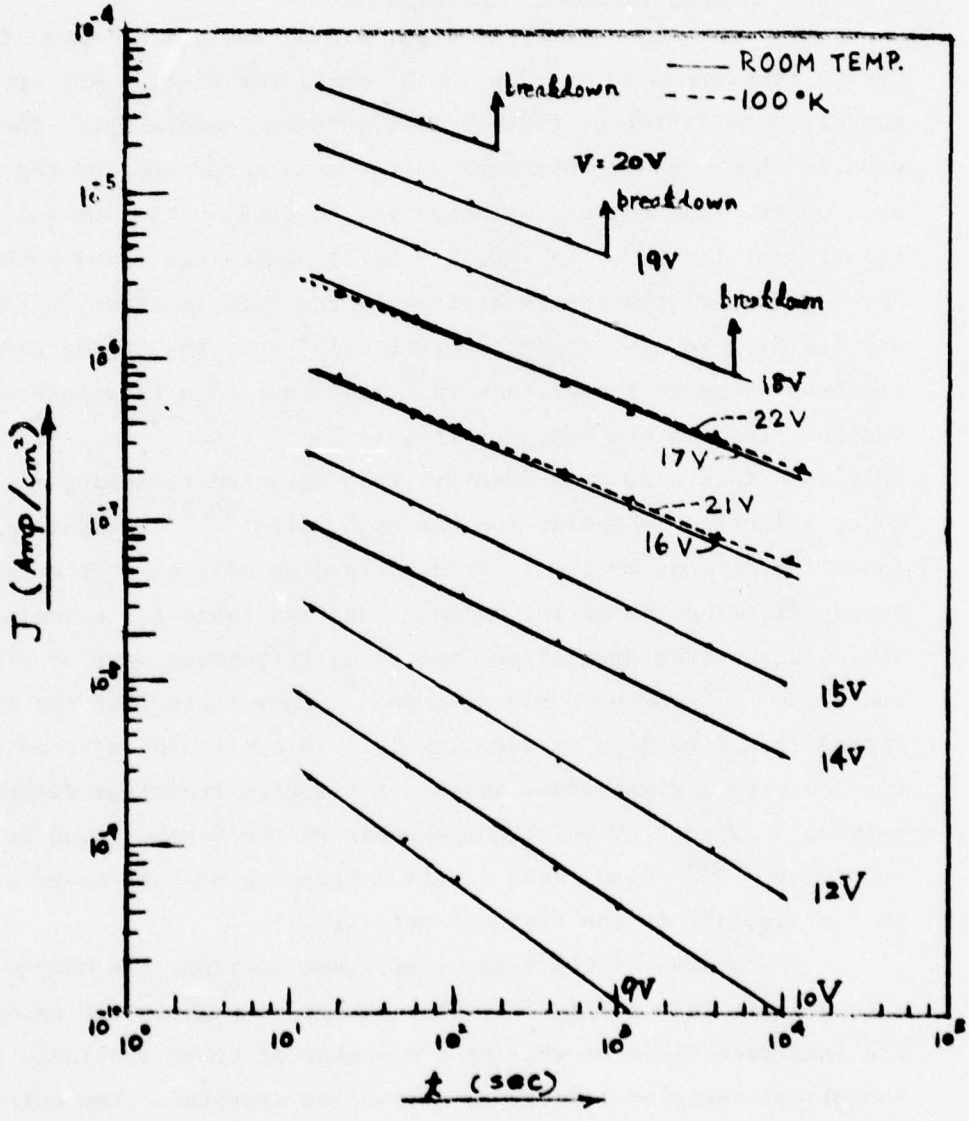


Fig. 4.1(a). Time dependence of current at various applied voltages for Si-450 Å Al_2O_3-Al structure. Solid curves: room temperature. Dashed curves: 98°K.

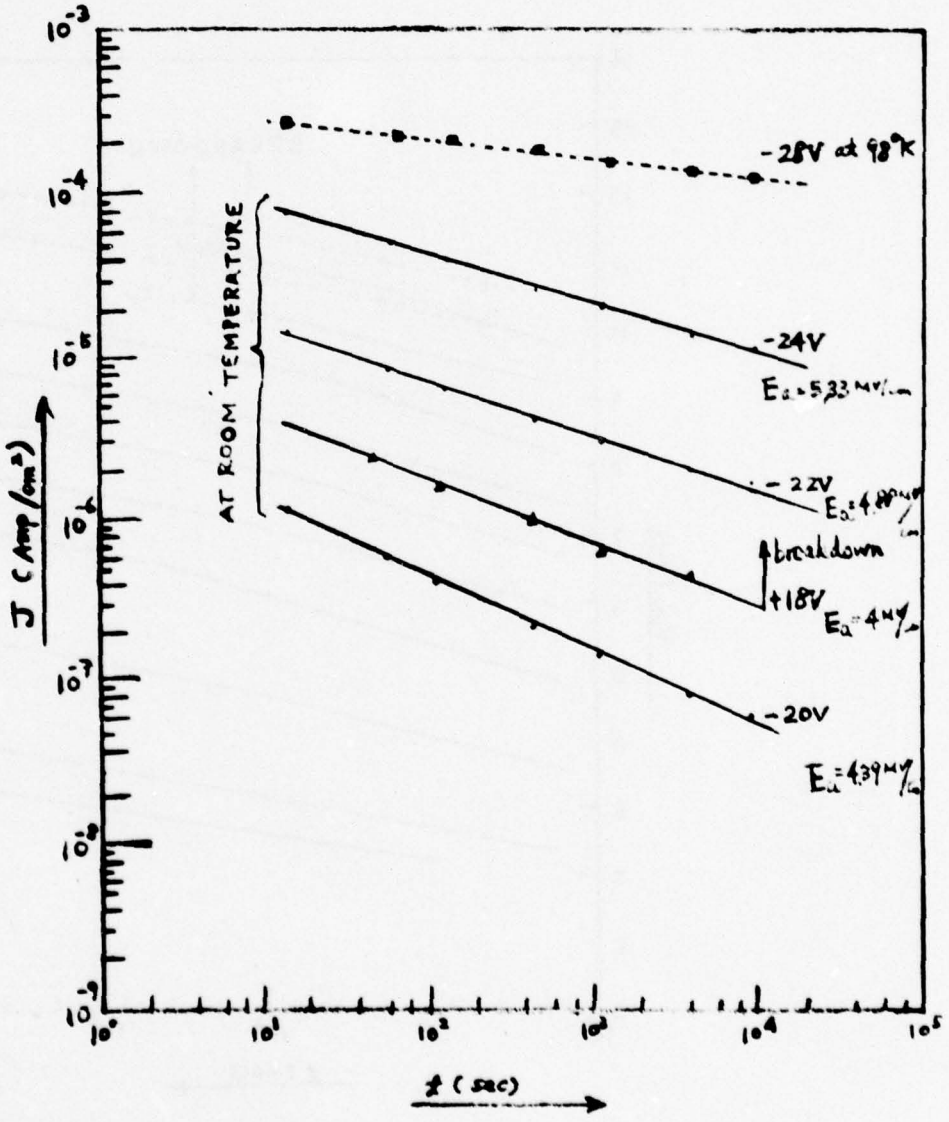


Fig. 4.1(b). Time dependence of current at various applied voltages for Si-450 Å Al_2O_3-Al structure [continued from Fig. 4.1(a)]. Solid curves: room temperature. Dashed curve: 98°K.

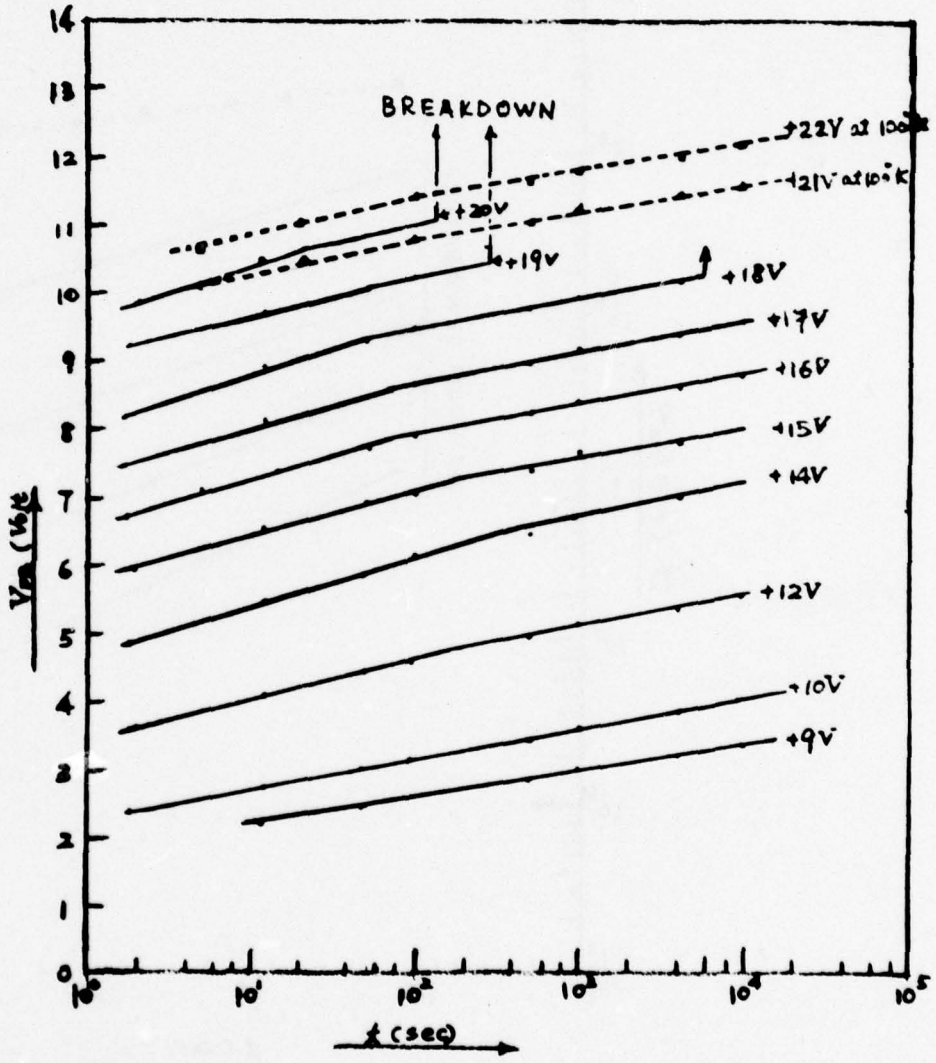


Fig. 4.2(a). Time dependence of flatband voltage for Si-450 Å Al_2O_3-Al structure. Solid curves: room temperature. Dashed curves: 100°K.

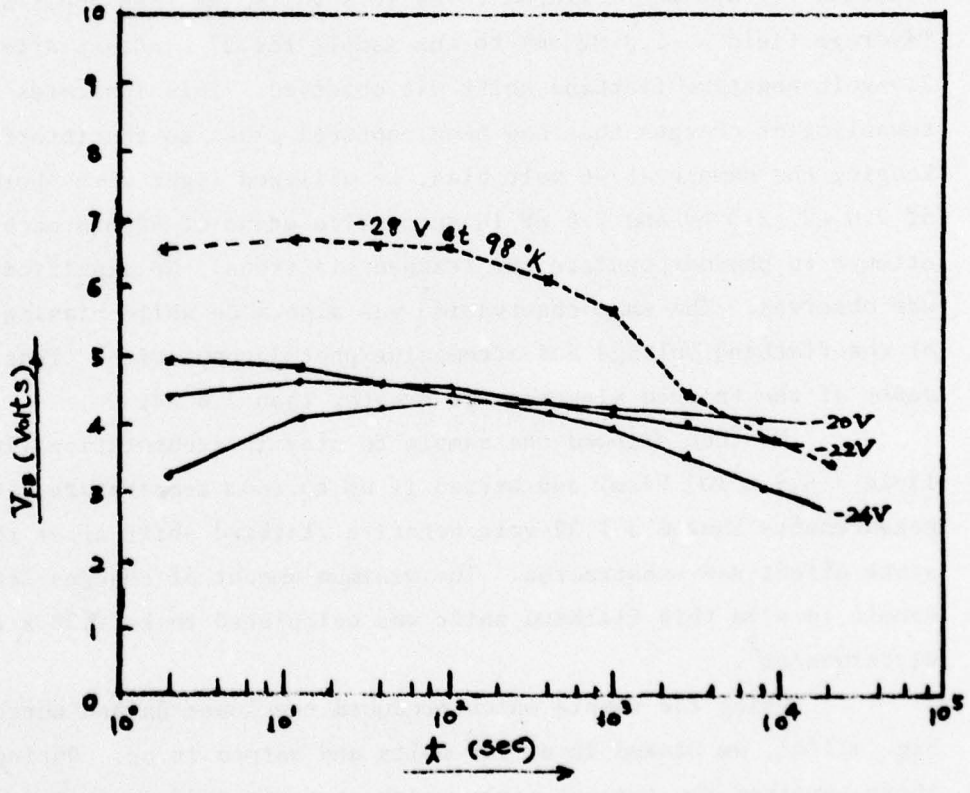


Fig. 4.2(b). Time dependence of flatband voltage for Si-450 Å Al_2O_3-Al structure [continued from Fig. 4.2(a)]. Solid curves: room temperature. Dashed curve: 98°K. The decrease in flatband voltage is due to hole trapping near the Si-Al_2O_3 interface.

Owing to the large barrier height between the electrode and the insulator,[50,51] the current will be limited by the injected carriers. However, as will be shown in the next section, we also found that trap-assisted conduction processes occurred in the bulk of the oxide.

4.3(B). Measurements at 98-100°K

The field stressing experiments were also performed on the Al-Al_2O_3-Si structures at 98-100°K. As is shown by the dashed curves of Fig. 1(a), the capacitors can sustain higher fields at low temperature, and the currents are smaller at a given voltage. This suggests that a thermally activated process is important in the transport mechanism in Al_2O_3. In order to investigate the temperature effect, we cooled the sample (which had a semitransparent gate) down to 94°K, and biased it to an average field of 4.67 MV/cm for 10 minutes. After stressing the flatband voltage was measured to be 10.5 volts. We then applied -6 volts (average field $\sim$ -1.3 MV/cm) to the sample for 27 minutes, after which a 2.4-volt negative flatband shift was observed. This indicates back-tunneling of charges that had been captured close to the interface. Keeping the sample at -6 volt bias, we utilized light with photon energies of 2.0 eV, 2.5 eV and 2.8 eV in successive steps of 40 min each in an attempt to photodepopulate the trapped electrons. No significant change was observed. The same observation was also made while biasing the sample at the flatband voltage and attempting photodepopulation. Thus the optical depth of the trapped electrons is greater than 2.8 eV.

We then allowed the sample to stay in accumulation (interface field = 8.9×10^5 V/cm) and warmed it up to room temperature. C-V measurements showed a 1.32-volt negative flatband shift after the interface-state effect was substracted. The minimum amount of charges lost by the sample to give this flatband shift was calculated to be 1.36×10^{12} electrons/cm^2.

Using the sample which produced the lower dashed curve of Fig. 4.1(a), we biased it at +16 volts and warmed it up. During warming there appeared two current peaks which strongly indicated thermal emission of trapped electrons.

On the other hand, we biased a p-type sample at -22 volt for 80 minutes, then cooled the system down. A 2-volt gain of flatband voltage was observed.

Direct tunneling via traps into the conduction band is a process that would be independent of the temperature.[52] The annealed charges which are not emitted by high field at low temperature must be detrapped by other processes. Since the density of electron traps is very large (average distance between traps less than 75 Å), it is very probable that a thermally activated hopping process can occur in the oxide. Poole-Frankel emission (thermal emission over a field-lowered barrier) may contribute to the decrease of charge storage, also.[53]

Three injection models for electrons are shown in Fig. 4.3. In all three, electrons tunnel from the negative electrode into traps. The charge carriers in the traps can be relaxed into the conduction band by (a) thermal emission, (b) tunneling,[40,54] or (c) thermally assisted tunneling. The charge trapping changes local band bending, which affects all of the tunneling processes.

4.4. High-Field Breakdown of Al_2O_3

The field strength of Al-Al_2O_3-Si is indicated in Figs. 4.1 and 4.2. It will be observed that most of the samples (450 Å in thickness) will break down within 10^4 sec under +18 volt or -25.5 volt bias. Although there were some variations from wafer to wafer in the average time needed to break down the oxide, the electronic properties of the various samples were found to be very similar.

4.4(A). Effect of Temperature

The breakdown strength of the Al_2O_3 samples was always higher (for the same stress time) at 100°K than at room temperature. As shown in Figs. 4.1(a) and (b), the samples sustained -28V and +22V for 10^4 sec at 100°K. The charge trapping is indicated by the results shown in Figs. 4.2(a) and (b). Because of the large barrier height between the silicon substrate and the Al_2O_3 valence band,[46,51] the hole injection level is expected to be very low. It is found that hole trapping, unlike electron trapping, increases gradually. We also indicated previously that there was electron trapping at low

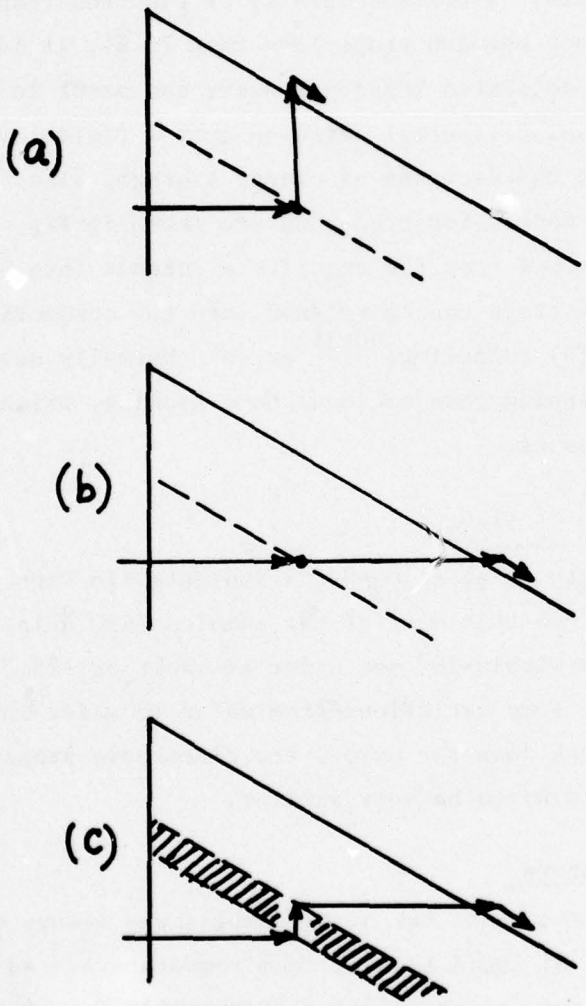


Fig. 4.3. Models of trap-assisted injection of electrons. (a) Tunneling into trap followed by thermal emission from the trap. The barrier for emission may be lowered by the Poole-Frenkel effect. (b) Trap-assisted tunneling. (c) Tunneling into trap followed by thermally assisted tunneling into the conduction band of the oxide.

temperatures. Therefore, it appears that the maximum localized field at 100°K is not less than at room temperature.

4.4(B). Self-Quenched Breakdown (SQBD)

We investigated the effect of negative field stress on Si-500 Å Al_2O_3-Au structures. The current vs. time at room temperature is shown in Fig. 4.4 for two bias voltages. Comparison with Fig. 4.1(b) shows that the current level for the Au gate is about two orders of magnitude smaller than for an Al gate at the same average field. The influence of the contact barrier height for electrons (4.1 eV for Au, 3.2 eV for Al)[50,51] on the current is quite prominent. Similar to the results obtained with negative corona charging, the C-V curves always show a negative flatband voltage.[1]

As is indicated in Fig. 4.4, self-quenching breakdowns began after 9×10^3 sec at -27 V (average field of 5.3 MV/cm). The breakdown rate was found to increase with time until the sample finally reached a state of high conduction. The breakdown spots for a sample with a p-type substrate are shown in Fig. 4.5. With the semi-transparent gate, a large area of gold around the breakdown spot can be vaporized. We also evaporated gold gates on the n-substrate sample used for Fig. 4.1(a). Self-quenched breakdowns were also observed in this sample under high negative bias. The samples with Al gates did not exhibit the self-quenching effect, although breakdown spots did appear on the gate, as shown in Fig. 4.6. It would seem that the breakdown occurred at a single localized spot.

4.5. Further Consideration of Breakdown Mechanisms

Our previous report[1] shows that with high negative bias, electron trapping occurs close to the front surface whereas hole trapping occurs near the Si-Al_2O_3 interface. With a gold gate, a -5V flatband shift occurs at a field of approximately -5.5 MV/cm. If all of the hole trapping were located near the interface, the concentration would be 4.33×10^{12} holes/cm^2. This high concentration again suggests that trap-assisted tunneling is the major injection mechanism.

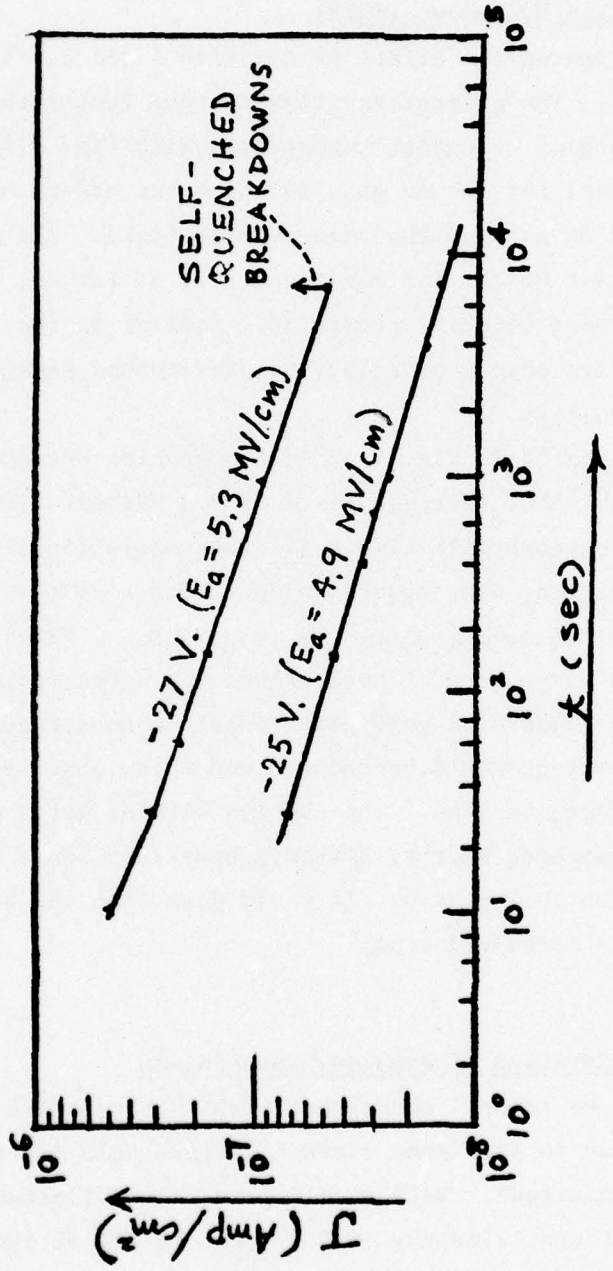


Fig. 4.4. Time dependence of the current for a Si-510 Å Al_2O_3-Au structure with negative bias. The current is much smaller than for an Al field plate [compare with Fig. 4.1(b)]. Self-quenched breakdowns begin after 9×10^3 sec at -27 V.

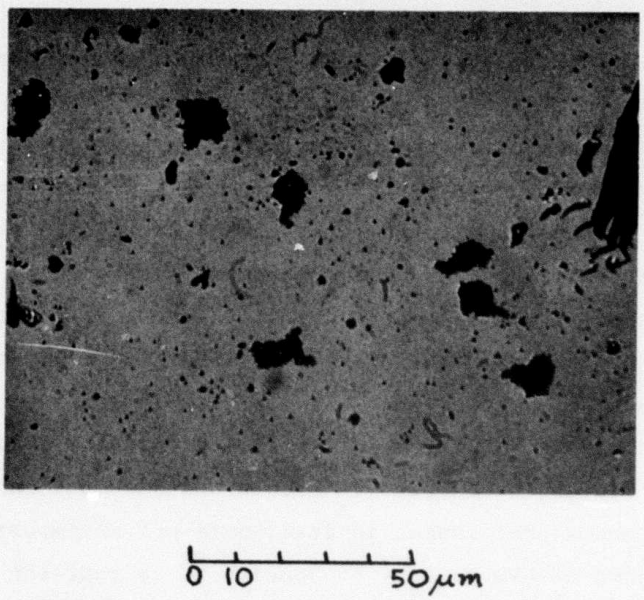


Fig. 4.5. Optical micrograph of self-quenched breakdowns. Structure: (100) p-Si/474 Å Al_2O_3/Au. Biased at -30V (field plate negative).

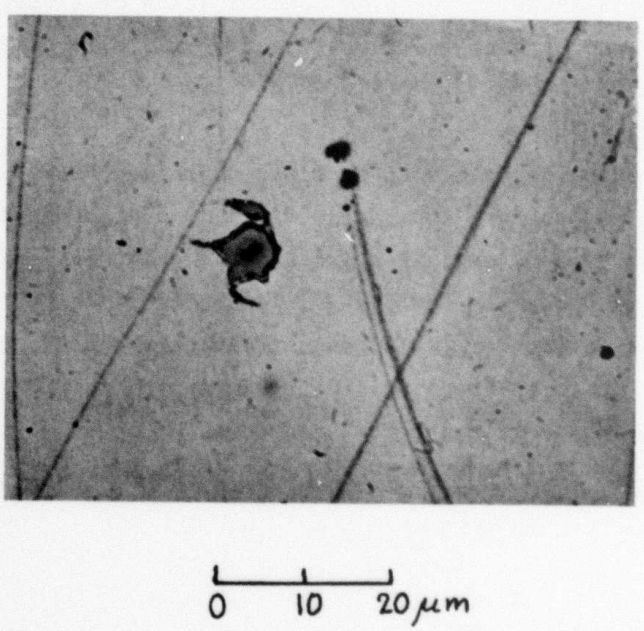


Fig. 4.6. Optical micrograph of breakdown spot obtained on an Al field plate. (100) p-Si/450Å Al_2O_3/Al. Breakdown voltage -30V (field plate negative).

Impact ionization depends very much on the mean free path of electrons between scattering events with optical phonons. At low temperatures the number of the optical phonons is reduced; thus the mean free path of the charge carriers is increased. If the breakdown originated from the impact effect, it would occur at lower fields at lower temperatures. However, our experimental results do not verify this expectation. We also reported that the mean free path between the electron and otpical phonons in Al_2O_3 is 4-5Å,[1,46-48] which is one-sixth of that in thermally grown SiO_2.[55-57] This again indicates that the number of hot electrons will be quite limited in Al_2O_3. We observed that even at high fields the current is stable and does not run away. It therefore seems that impact ionization is not an important factor in the breakdown of CVD Al_2O_3. It appears to us that the instability leading to high-field breakdown may be explained on the basis of field-dependent shallow and deep trapping, and the influence of the field-dependent trapped charge on the charge-carrier injection.

4.6. Summary

(1) Because of the high concentration of electron and hole traps in the Al_2O_3, charge-carrier injection is believed to be domianted by trap-assisted tunneling.

(2) The bulk traps can also contribute to the conduction mechanism through the processes of field tunneling, Poole-Frenkel emission, and perhaps a temperature-activated, field-dependent hopping process.

(3) Present estimates indicate that impact ionization is not an important mechanism in the high-field breakdown of CVD Al_2O_3 on Si.

(4) Future work will concentrate on the study of the characteristics of the electron trapping and hole trapping in the Al_2O_3, and on deducing a satisfactory model for breakdown.

5. INVESTIGATION OF HIGH FIELD EFFECTS IN Al-Al_2O_3-Si CAPACITORS

(O. Bar-Gadda collaborating)

We report here on the continuation of experiments relating to charge storage and dielectric breakdown in Al_2O_3 on silicon substrates.

5.1. Samples

Our samples were fabricated at Bell Laboratories through the courtesy of G. E. Smith and D. M. Boulin. The substrates were both p-type and n-type (100) 4-6 ohm-cm silicon. The Al_2O_3 films were CVD deposited at temperatures of 815 and 900°C to thicknesses in the range 450-550 Å. Various kinds of field plates were used: 1000-Å Al, 200-Å Al, and 1000-Å Au.

5.2. I-V Characteristics

We have measured the I-V characteristics of the Al-Al_2O_3-Si capacitors. The difficulties encountered are two: (1) The large amount of electron trapping causes the oxide field to change rapidly, and therefore the current also. (2) On application of a voltage pulse, there is a capacitive displacement-current transient in addition to the injection current. These difficulties we attempted to overcome by use of the circuit in Fig. 5.1. The value of the capacitor C is adjusted to equal the accumulation capacitance of the sample. We measure the voltage difference $V = V_1 - V_2 = (I_s + I_t)\,R - I_tR = I_sR$ where I_s is the injection current, I_t is the transient displacement current. Therefore, use of this circuit effectively eliminates the transient displacement effect. If the current I_s is recorded on an oscilloscope by measuring the voltage $V = I_sR$, the value $I_s(t = 0)$ gives the injection current for applied field $E_a = V_a/d$. In practice, it is difficult to cancel entirely the transient effects, and therefore the current is determined at $t = 0^+$ (< 1 μs). Also, the sample-to-sample variations give a scatter in the values. Nevertheless, the resulting I-V curve is useful in getting an order-of-magnitude estimate of the current densities involved. Figure 5.2 shows J-V curves obtained from these measurements. At very high fields, the data may not be completely reliable because significant injection takes place at very small times. The low-field result compares favorably with that of Powell and Hughes.[40] Note that at breakdown fields

Fig.51. Circuit for measurement of I-V characteristics

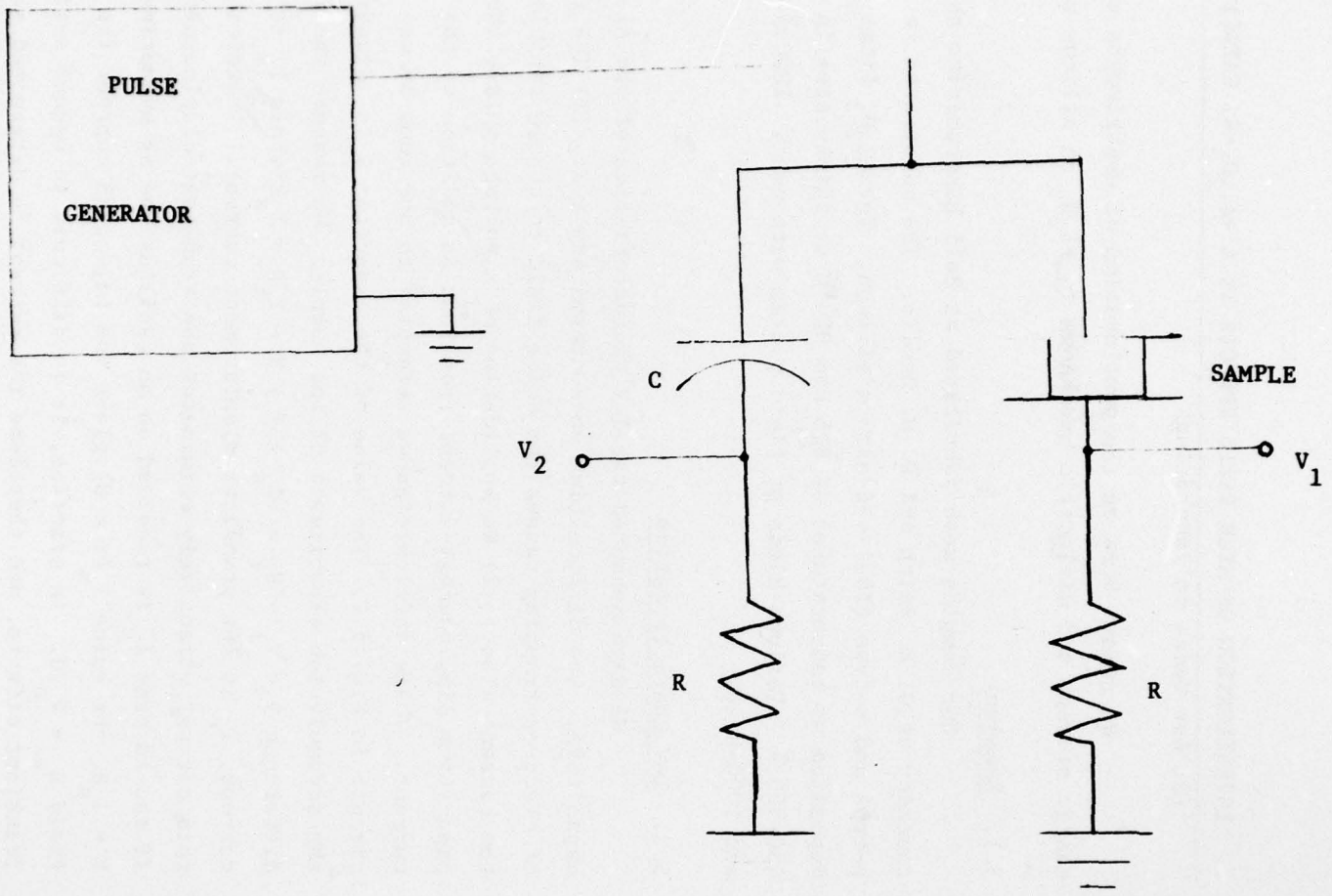


Fig. 5.2(a) J-V characteristics for positive bias on n-Si (Al gate, 450 Å Al_2O_3)

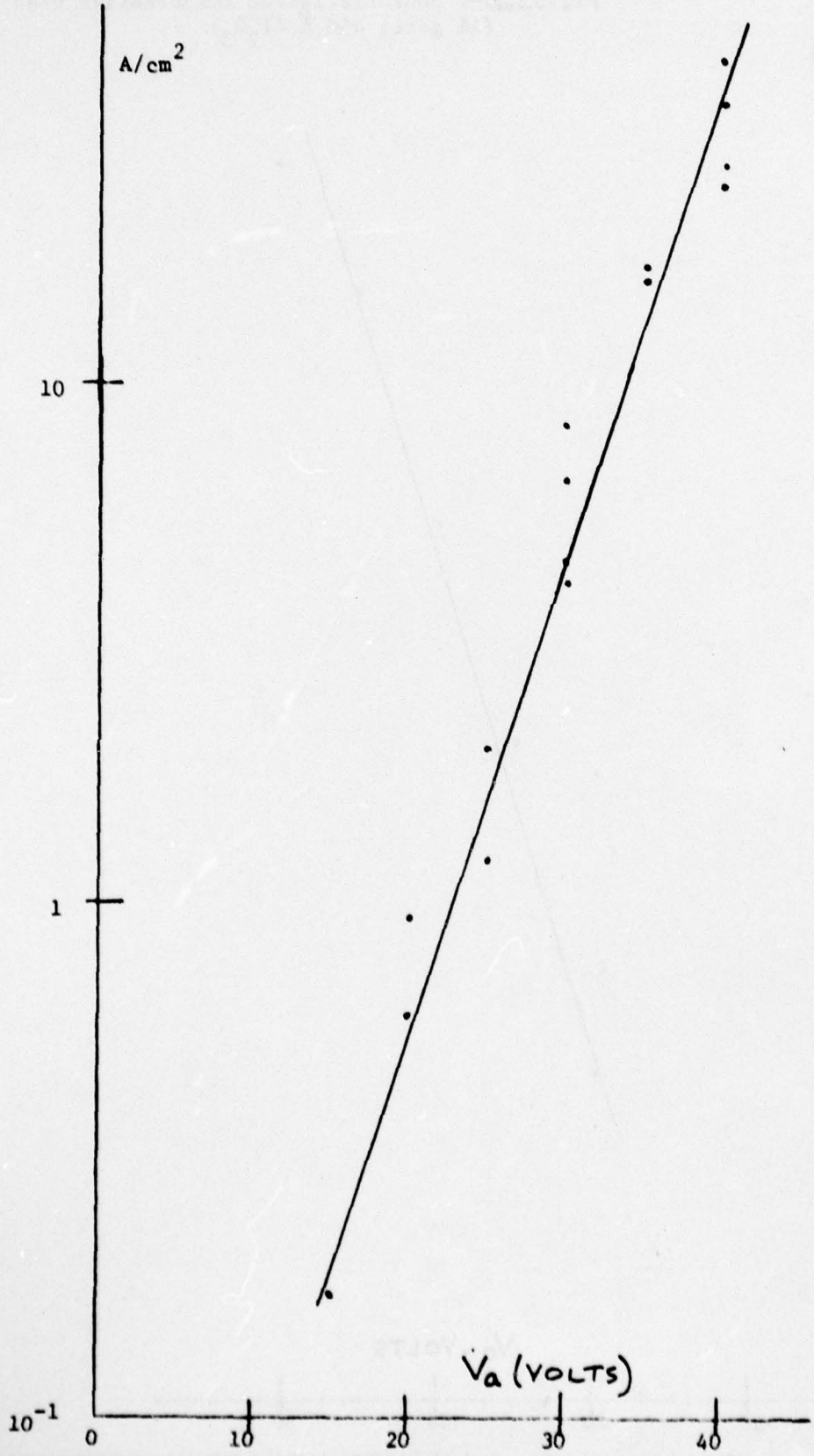
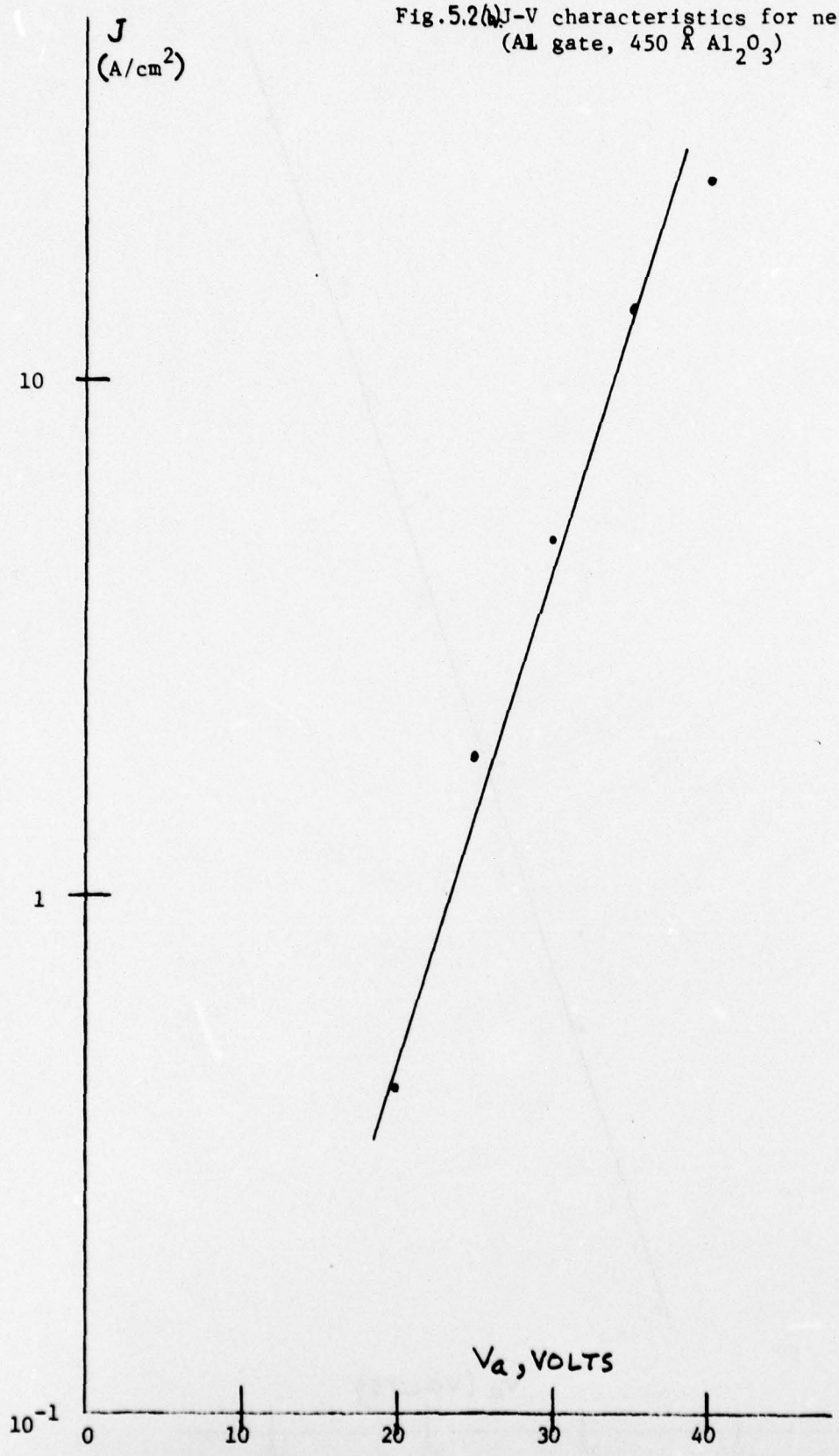


Fig.5.2(b) J-V characteristics for negative bias on p-Si (Al gate, 450 Å Al_2O_3)



($\gtrsim$ 5 MV/cm) we have J $\gtrsim$ 1 A/cm^2.

5.3. I-t Characteristics

We have studied the I-t behavior for both short and long times. The large-t behavior is shown in Fig. 5.3. For both polarities, the current is seen to approximate a $1/\sqrt{t}$ behavior at large t. A calculation of McLean et al,[58] based on a single energy level trap, predicts a 1/t behavior. However, Harari and Royce[44] have shown that there are several trapping bands. Also, the existence of both electron and hole traps rules out any simple model of the trapping, even if it predicts correctly the logarithmic time dependence of the trapped charge.

5.4. ΔV_{FB}-t Characteristics

We have studied the ΔV_{FB} vs. t characteristics for times up to 10^4 seconds. For positive bias on n-type substrate, we see that the logarithmic behavior is maintained [Fig. 5.4(a)]. For negative bias on p-Si, the flatband shift reversal is clearly seen for applied fields above 4 MV/cm [Fig. 5.4(b)]. This is believed due to hole trapping near the Si interface. The probability of hole trapping is also strongly suggested by Fig. 5.4(c), which shows the results of negative bias on p-type Si with Au electrode and 500 Å Al_2O_3 film. The higher barrier height of gold reduces electron injection at the cathode. Below about 4 MV/cm, one can detect a slight positive flatband shift. Above 4 MV/cm one observes a negative flatband shift, consistent with a model of hole injection and trapping.

5.5. Model of Trapping

In order to get an order-of-magnitude estimate we construct a very simplified model. Assume a uniform trap density N traps/cm^3. Let us also assume that for the case of the applied field equal to the breakdown field, the internal bulk field at breakdown is about the same for both polarities. Since the applied fields are approximately equal, and assuming only electron trapping near the cathode, then the amount of charge trapping is the same for both polarities, which implies that the relative location of the charge centroid is also the same. Then we have

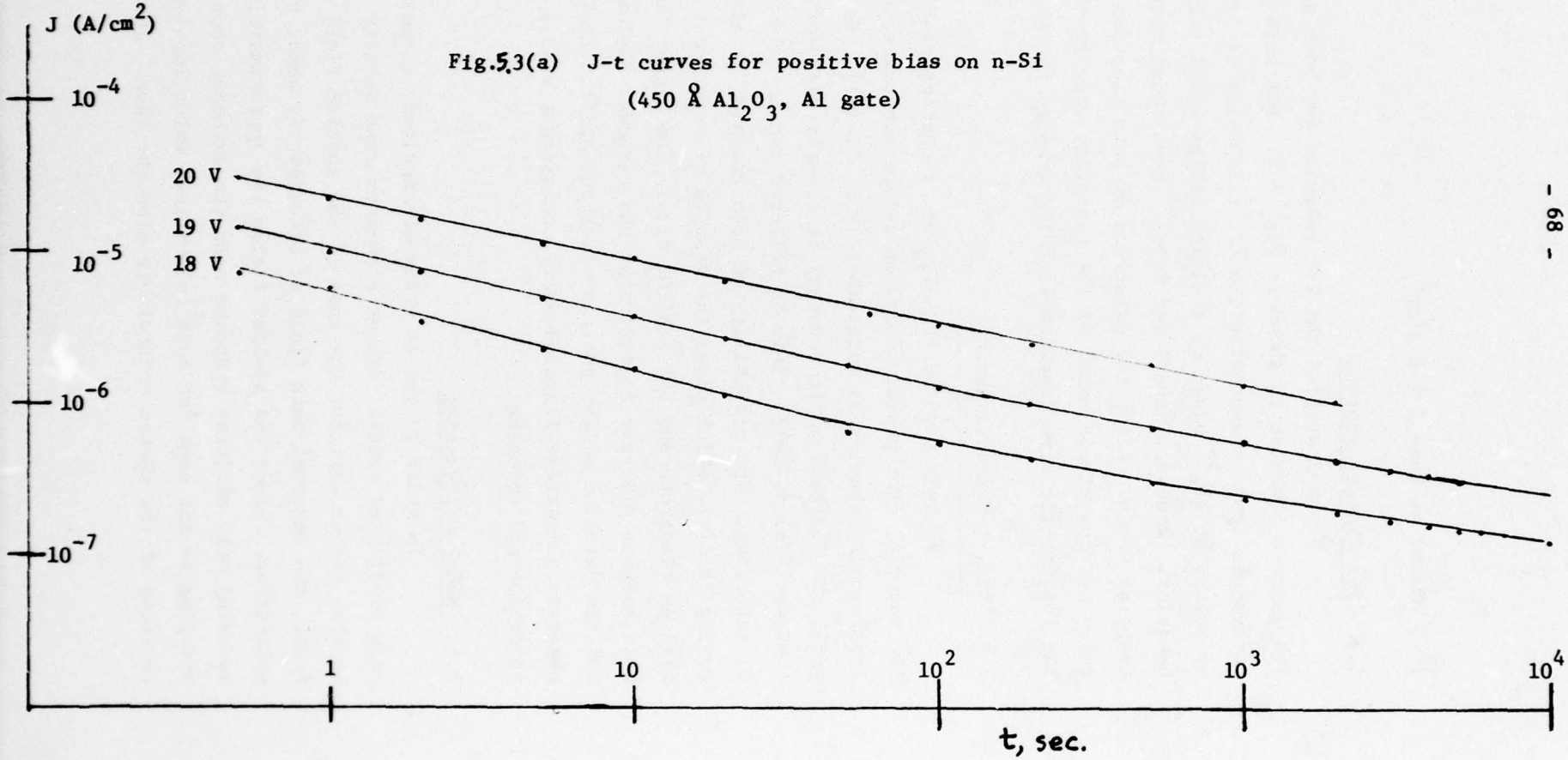


Fig.5.3(a) J-t curves for positive bias on n-Si
(450 Å Al_2O_3, Al gate)

Fig.5.3(b) J-t curves for negative bias on p-Si
(450 Å Al_2O_3, Al gate)

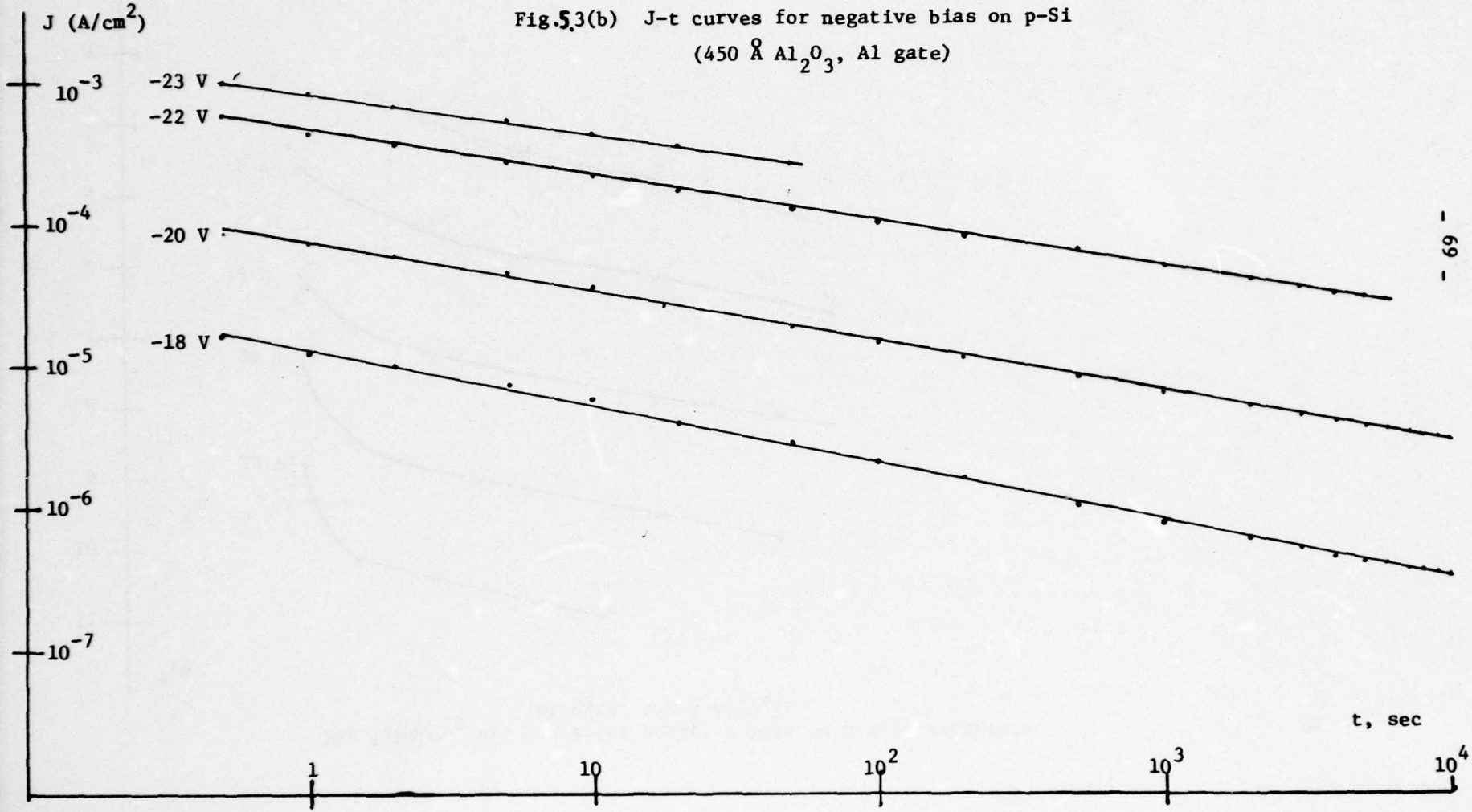


Fig. 5.4(a). V_{FB} vs. log t for positive bias on n-type substrate (Al gate, 450 Å Al_2O_3)

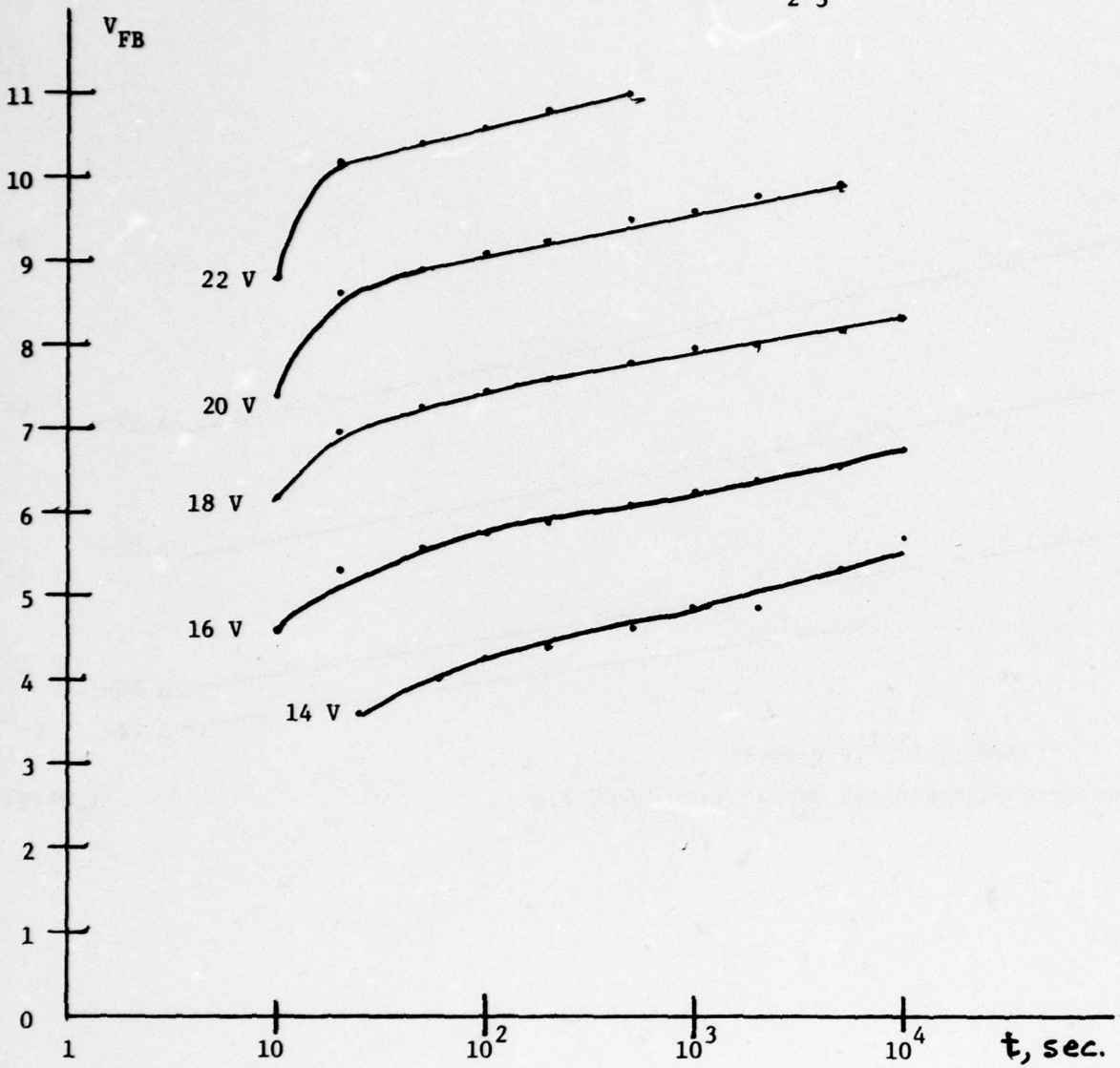


Fig.5.4(b) V_{FB} vs. log t for negative bias on p-type substrate
(Al gate, 475 $\underline{\text{Å}}$ Al_2O_3)

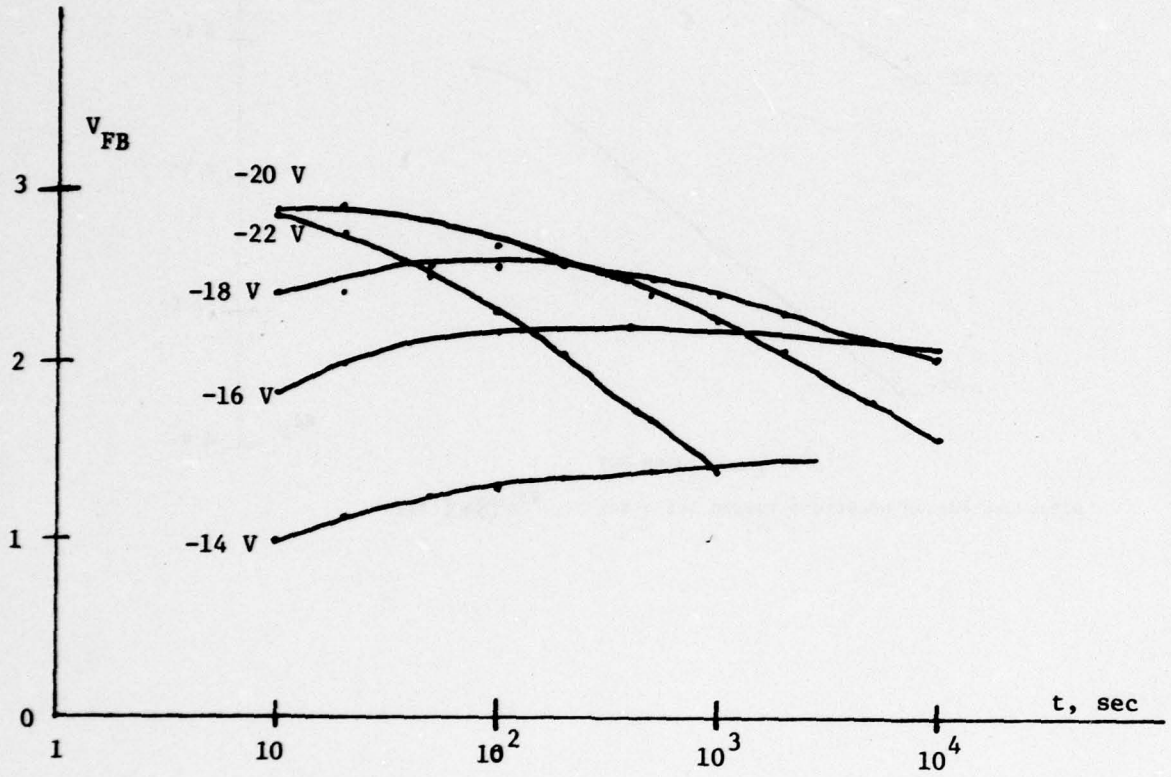
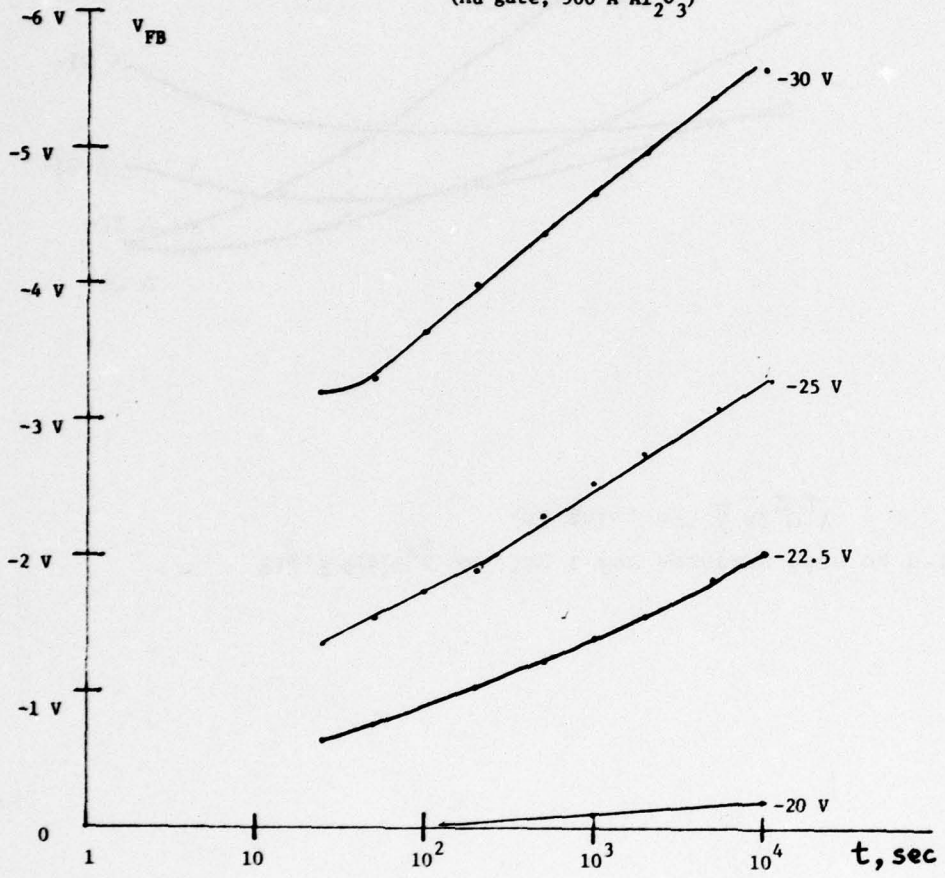


Fig. 5.4(c). V_{FB} vs. log t for negative bias on p-type substrate

(Au gate, 500 Å Al_2O_3)



$$\Delta V_{FB(-)} = \frac{Q_{T(-)}\bar{x}}{C_o x_o}, \quad \Delta V_{FB(+)} = \frac{Q_{T(+)}(1 - \bar{x}/x_o)}{C_o}$$

$$Q_{T(-)} = 2eN\bar{x}, \quad Q_{T(+)} = 2eN\bar{x}$$

$$\Delta V_{FB(-)} = \frac{2eN\bar{x}^2}{C_o x_o}, \quad \Delta V_{FB(+)} = 2eN\bar{x}(1 - \bar{x}/x_o)C_o$$

$$\frac{\Delta V_{FB(-)}}{\Delta V_{FB_{(+)}}} = \frac{\bar{x}^2/x_o}{\bar{x}\,(1 - \bar{x}/x_o)} = \frac{\bar{x}/x_o}{1 - \bar{x}/x_o}$$

$$\frac{\bar{x}}{x_o} = \frac{\Delta V_{FB(-)}/\Delta V_{FB(+)}}{1 + \Delta V_{FB(-)}/\Delta V_{FB(+)}}$$

Using $\Delta V_{FB(-)} = 3.7$ V and $\Delta V_{FB(+)} = 7$ V, we obtain $\bar{x}/x_o = 0.35$ and $\bar{x} = 160$ Å. This calculation, although crude, shows that trapping takes place through much of the bulk of this thin oxide. The trapping density is computed approximately as $N = \frac{\Delta V_{FB(-)} C_o x_o}{2e\bar{x}^2}$. Substituting $\Delta V_{FB} = 3.7$ V, $C_o = 400\text{pF}/2 \times 10^{-3}$ cm^2 and $\bar{x}/x_o = 0.35$, we obtain $N = 4 \times 10^{18}$ traps/cm^3. This gives the number of occupied traps, and thus the actual trap density may be much higher. This figure is about an order of magnitude lower than reported by McLean et al.[58] As an interesting sidelight, application of the above calculation technique to the results of Powell and Hughes[40] gives a value of $\bar{x} = 100$ Å for $x_o = 1100$ Å. This would suggest that most of the trapped charge does lie near the interface, but for a thin oxide it would appear to be distributed more uniformly.

5.6. Breakdown Damage

Breakdown damage has been studied. Here we show optical and scanning electron micrographs. Figure 5.5 shows an optical micrograph of breakdown caused by negative bias on p-Si, with a 1000 Å Al electrode.

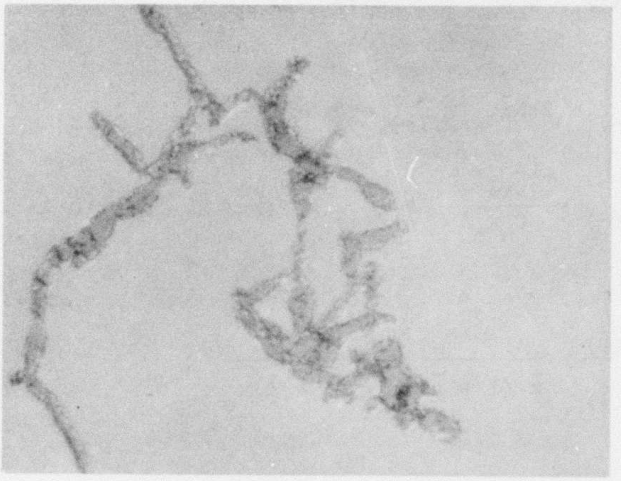


Fig. 5.5. Optical micrograph of typical breakdown damage. p-Si substrate, -22.5V.

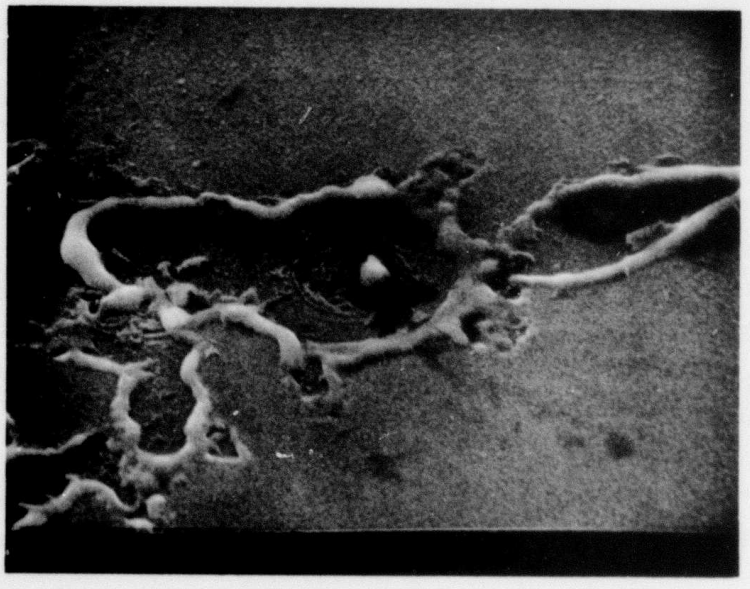


Fig. 5.6. Scanning electron micrograph corresponding to Fig. 5.5.

Figure 5.6 shows the corresponding scanning electron micrograph of the same area. Each of these pictures shows a region where the Al electrode appears to have been exploded away. In the center of the breakdown region of the SEM pictures is a white dot. This may be molten Si, molten Al_2O_3, or a mixture of the two. It may be this white dot which is associated with a filamentary conduction process. Another structure seen on breakdown shows portions of the Al which have not been exploded away but have instead been crumpled into a series of ridges and rippled areas. Figure 5.7 shows a ridged, branching structure for breakdown on an n-type substrate. For n-type substrates, it was usually very difficult, if even possible, to locate breakdown spots on 1000 Å Al dots. For 200 Å Al gates, though, structures similar to those shown in Fig. 5.7 are always seen after breakdown.

The location of the breakdown spots was predominantly, although not exclusively, near the edge of the dot. However, there is no correlation between the distance of the breakdown spot from the center of the dot and the time to breakdown.

The effect of ions is probably small. In one experiment, a sample was immersed in deionized water for 11 days at room temperature. Although the Al electrodes suffered noticeable degradation, the samples showed negligible flatband shift and no measurable change in breakdown strength.

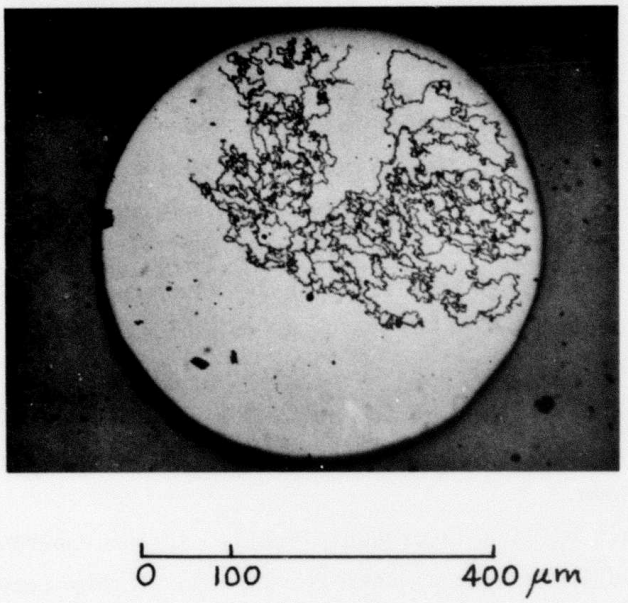


Fig. 5.7. Optical micrograph of typical breakdown damage. 200-Å Al field plate, +27V.

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